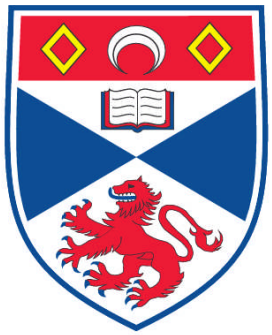
SILICON ELECTRO-OPTIC MODULATOR

Fengqiao Dong

A Thesis Submitted for the Degree of MPhil
at the
University of St. Andrews



2011

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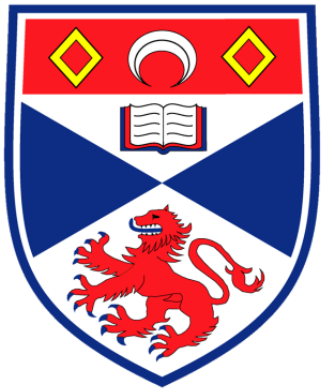

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This thesis is submitted in partial fulfilment for the degree of MPhil at the University of St Andrews

September 2011

For my parents

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Acknowledgement

I would like to thank my supervisor, Prof. Thomas F. Krauss, who has guided me and helped me as much as he could during my study in St Andrews.

I also would like to thank Dr. William Whelan-Curtin (also known as Dr. Liam O'Faolain), Dr. Juntao Li and Dr. Timothy D. James for the knowledge they have shared with me and many useful discussions we have made. My special thanks to Dr. Timothy D. James for proof reading this thesis. I sincerely appreciate all the time they have spent on this work. I thank Mr Steven Balfour for keeping the cleanroom in order.

Finally, I would say without the help from the members of the group, it would be impossible for me to complete this project. They have made the research so enjoyable.

Abstract

In recent years, as on-chip data transmission has increased dramatically, much time and effort has been devoted to the development of compact electro-optic modulators with large bandwidth and low power consumption, which is the key component for on-chip data links. Silicon which has been widely used in electronic industry has been considered as a promising material for electro-optic modulators, due to its mature manufacturing technology and low cost.

In this work, a silicon electro-optic modulator based on a new type of phase shifter is proposed. The phase shifter is in one arm of an asymmetric Mach-Zehnder interferometer (MZI) structure and operates very similar to a MOS capacitor. Indium tin oxide (ITO) is used as an electrode and flowable oxide (FOx, spin-on-glass) is used as a gate oxide. ITO is being widely used in many electro-optic applications as a transparent conductor, as it offers both electrical conductivity and optical transparency, although it has seen less use in optical waveguide devices.

Electrical simulations have been completed in order to study the electrical performance of the phase shifter and also to improve the design. SiO_2 has been used as a gate oxide in the simulation. The depletion region width and capacitance-voltage (C-V) characterization have been modelled. Based on the theoretical analysis and simulation results, n-type silicon with the doping concentration of 1×10^{17} cm^{-3} has been chosen as the active material.

ITO fabrication and its electrical and optical properties have been studied. The effect of ITO annealing on sheet resistance and transmittance has been investigated. ITO (140 nm thick) annealed at 400˚C for 30 minutes in air shows the best result. The sheet resistance is around 750 Ω/□ and the optical transmittance is about 87%.

Aluminium (Al) electrical contacts to silicon have been fabricated and tested. The HF cleaning and post thermal annealing effect on the contact resistance has been investigated. The transmission line method (TLM) has been used to determine the contact resistance. The Al contact resistance is about 335 Ω on n-type silicon substrate with a doping concentration of 1×10^{17} cm^{-3}.

ITO-FOx phase shifters and modulators have been fabricated and tested. The MZI structure of the modulator shows the typical interference pattern. This is important for realising phase-intensity modulation. Al-FOx phase shifters have also been fabricated and tested. The transmission depends on the Voltage, both in terms of phase and the optical loss, clearly indicating a change in carrier density. Although ITO-FOx phase shifters and modulators did not work successfully due to high optical losses caused by waveguides sidewall roughness and fabrication process, ITO showed promise to use in electro-optic modulators as a transparent conducting layer. The ITO layer separates silicon waveguides from Al contacts and lowers optical losses due to metal absorption.

Overall, successful operation of a MOS-capacitor type optical phase shifter has been achieved, but the modulation efficiency is low (1 dB at 50 V) and the insertion loss is high (over 10 dB).

Contents

List of Figures

List of Tables

Chapter 1

Introduction & Theory

Silicon electro-optic modulator overview

The demand for large data transmission is continuing to increase exponentially. Network interconnects, for both conventional data networks and inter-chip data links, continue to scale in complexity and bandwidth year after year [1]. Because transistors are getting smaller and more compact, the resistance of copper interconnects and transmission delays increases dramatically when copper wires decrease to sub 90 nm dimensions [2]. Besides, the power consumption increases with the data transmission speed in copper interconnects. In order to meet this increasing demand and tackle the problem with copper, photonic devices have been introduced into telecommunication and on-chip data links for high speed processing [3]. Many types of photonic devices have been proposed and developed

using a variety of materials, such as $LiNbO_3$ [4,5] and III-V semiconductor compounds [6,7]. The leading candidate technology is silicon photonics [8].

Although electro-optic modulators based on $LiNbO_3$ and III-V semiconductor compounds have already been commercially available at speeds up to 40 Gb/s, silicon electro-optic modulators show more promise in terms of future integration with silicon electronics in a cost-effective manner. The state-of-the-art silicon electro-optic modulator is based on a MZI interferometer with a reverse biased PN junction in both of the arms, achieving a high speed of 40 Gb/s with 20 dB extinction ratio and an insertion loss of 7 dB. The length of this device is over 1 mm. In order to have small RC constant, traveling-wave electrodes which allow electrical and optical signal co-propagation along the waveguide and therefore keep the RF attenuation low have been used in the modulator [42].

The three critical issues in silicon electro-optic modulator research are RC time constant, optical insertion loss and size of the device. RC time constant ultimately limits the modulation speed and can be lowered by designing the device with smaller capacitance and resistance [42]. Insertion loss limits the optical performance of the modulator. It can be reduced by using silicon waveguides with low doping concentrations to lower the free carrier absorption loss. Also, a layer of transparent conducting material can be used to keep metal contacts away from silicon waveguides so as to reduce the optical losses due to metal absorption [26]. The size of the device relates to integration with other devices and also cost. Enhancement techniques such as slow light photonic crystal (PhC) waveguides and ring resonators can be used to reduce the device footprint. Our goal is to achieve

similar performance to the state-of-the-art silicon electro-optic modulator with a shorter length (<100 um) by using slow light PhC waveguides. The electrical performance, especially the depletion region width and capacitance, has been investigated and simulated. ITO as a transparent conducting oxide has been investigated. And the optical loss due to the ITO film has been measured.

Although ruling the electronic industry for decades, silicon was not widely used in photonic devices initially, due to its own limitations, which includes high propagation losses (because of scattering induced by waveguide sidewall roughness), low electro-optic coefficient, low light-emission efficiency, and high fibre-to-waveguide coupling losses [9]. However, silicon has some excellent material properties that are important for photonic devices, that have now been recognised and studied, such as high thermal conductivity, high optical damage threshold, and high third-order optical nonlinearities [10]. Moreover, light absorption in silicon waveguides can be neglected, which means silicon is a transparent medium to guide light [11]. Another important reason of using silicon in photonic devices is that these devices are highly compatible with mature CMOS manufacturing technology, which can greatly reduce the cost compared with the devices based on other photonic materials [12]. At the same time, silicon is a good platform for ultra-compact monolithic integration of both electronic and photonic components [13]. These advantages have attracted much effort on developing silicon photonic devices. The origins of silicon photonics can be traced back to the fundamental works of Soref and Petermann et al. more than twenty years ago [14-18]. With the progress of nanofabrication techniques and other further investigations [19-22], a variety of

ultra-compact high-performance photonic devices based on silicon have been demonstrated. The first continuous silicon laser was reported in 2005 by Intel [23]. Low-loss silicon photonic waveguides with propagation losses down to 1 dB/cm [24] and even lower ~0.3 dB/cm [25] have been demonstrated. Silicon electro-optic modulators, as one of the key components for optical interconnects and photonic integrated circuits (PICs), have also been developed with compact size, high modulation speed and small power consumption [26-28, 42-45, 47].

In order to realize optical intensity modulation, silicon electro-optic modulators could be either based on the absorption mechanism or the phase shift mechanism. As silicon itself is transparent at the telecommunication wavelengths, absorption based modulators depend on either some external material which must have electrically controlled absorption–transmission properties, such as graphene [46], or a special designed structure that can control and modulate optical losses, such as ring resonators [27,45]. However, ring resonators need precise fabrication and high environment thermal stability due to their own limitations [8]. Besides, their bandwidth is relatively small [48]. Therefore, modulators based on phase shift converting to intensity change are much easier to realize and fabricate using the Mach-Zehnder (MZI) interferometer structures.

In a MZI structure, phase shifts in the arms can be converted to an intensity change of the output light. Realising electrically modulated phase shift becomes the key issue of the design of silicon electro-optic modulators.

1.2 Mach-Zehnder interferometric modulation structure

The Mach-Zehnder interferometer (MZI) (see Fig.1.1), invented in 1891 by physicists Ernst Mach and Ludwig Zehnder, has been widely used in many optical applications. The Mach-Zehnder interferometer is also an ideal optical structure to convert phase change into intensity change [49]. As in principle, it is simple and easy to fabricate, a number of optical modulators based on different materials have adopted the MZI structure. A typical MZI structure contains four precisely aligned optical elements: one beam splitter, one coupler and two mirrors. A schematic diagram of a basic MZI structure is shown in Fig.1.1.

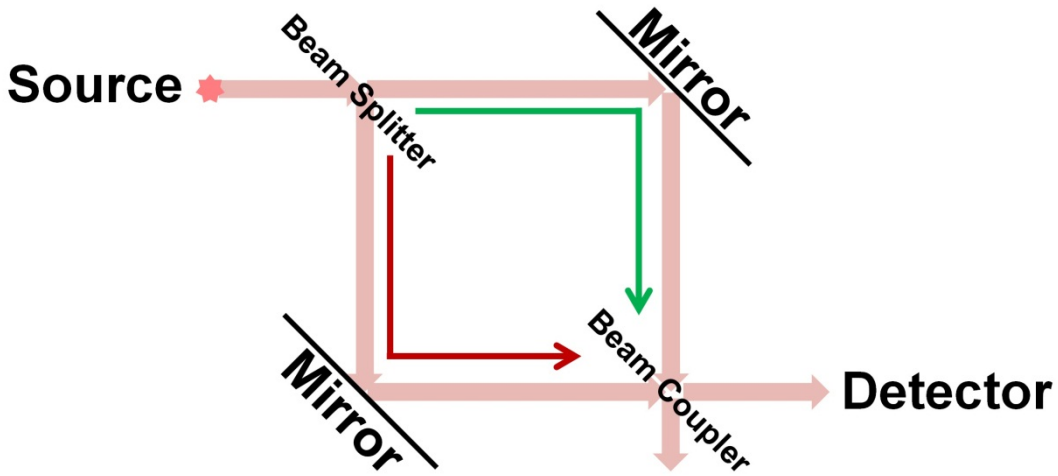


Fig.1.1 Mach-Zehnder interferometer. A typical MZI interferometer contains four elements: one beam splitter, one coupler and two mirrors. The input light is split into two arms and recombined to have interference.

The light is divided into the two arms at the input splitter, and later they are recombined at the output coupler. The two arms of MZI can be symmetric or

asymmetric in optical path. The asymmetric MZI structure may be more sensitive to changes in refractive index than the symmetric one [50], when it is working in the "critical coupling". Besides, the output light intensity of an asymmetric MZI structure is also wavelength dependent [49]. Therefore, the asymmetric type is a better platform as a starting point for phase-intensity modulation, where it is easier to observe a phase shift.

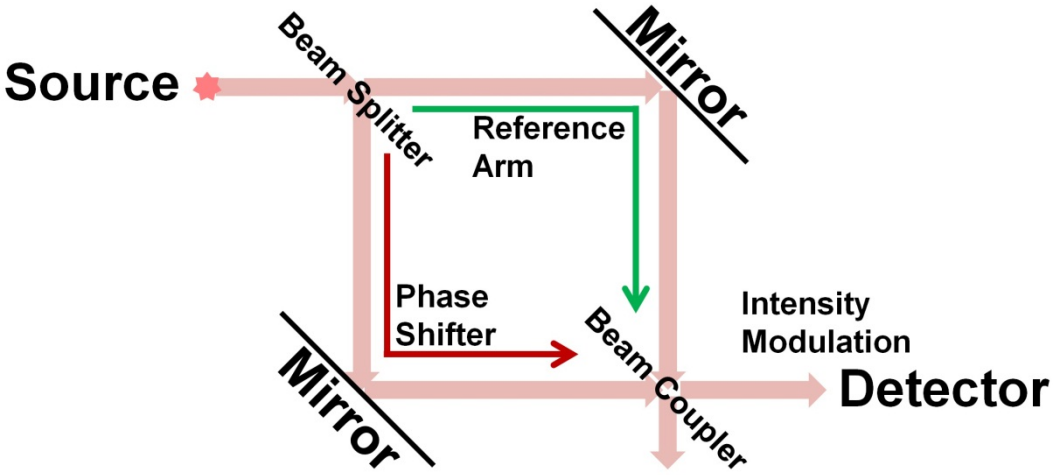


Fig.1.2 Asymmetric MZI structure for phase-intensity modulation. One arm is the phase shifter arm, the other one is the reference arm where there is no phase change. When the light with a phase shift combines with the unperturbed light, the total output intensity is also changed.

A typical asymmetric MZI structure for optical intensity modulation is shown in Fig.1.2. An optical signal is split equally by the beam splitter. The light travelling through the phase shifter arm is modulated and produces a phase shift Δφ, while the

light travelling through the other arm does not experience any phase change. The corresponding expressions for the optical fields in the two arms can be described as:

$$E_{TE1} = (A/2)\exp[i(\omega t + \Delta\varphi_1)] \quad \textbf{(0.1)}$$

$$E_{TE2} = (A/2)\exp[i(\omega t + \Delta\varphi_2)] \quad \textbf{(0.2)}$$

where A is the amplitude of input light, $\Delta\varphi_1$ and $\Delta\varphi_2$ are the phase changes experienced by the light as it propagates through the two arms. E_{TE1} and E_{TE2} are the optical fields in the phase shifter arm and the reference arm, respectively. We assume that the amplitudes in the two arms are equal and not affected by the phase change.

At the coupler, the light from the two arms interferes and recombines, and then the intensity of the output light is

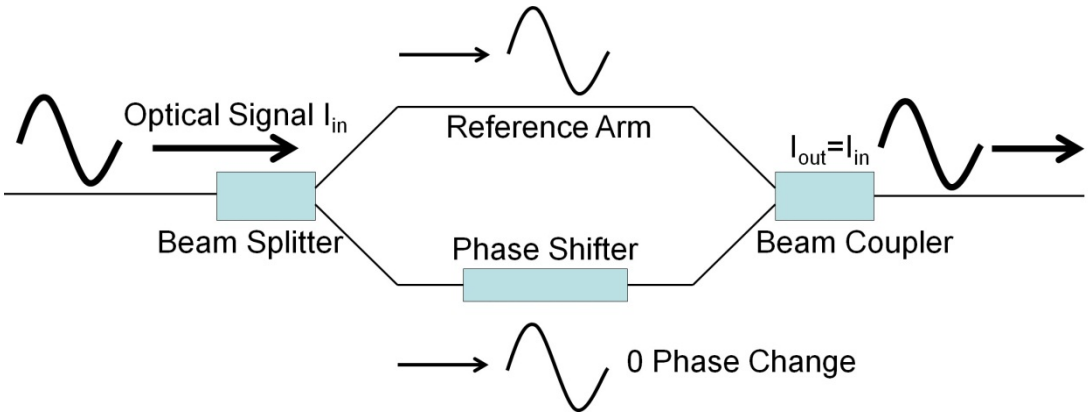
$$\begin{aligned} I_{out} &= \left|(A/2)\exp[i(\omega t + \Delta\varphi_1)] + (A/2)\exp[i(\omega t + \Delta\varphi_2)]\right|^2 \\ &= A^2\cos^2\left(\frac{\Delta\varphi_1 - \Delta\varphi_2}{2}\right) \\ &= I_{in}\cos^2(\Delta\varphi/2) \end{aligned} \quad \textbf{(0.3)}$$

where $\Delta\varphi = \Delta\varphi_1 - \Delta\varphi_2$ is the total phase difference between the two arms. The light in the reference arm does not have any phase change $\Delta\varphi_2 = 0$. According to the trigonometric theory $\cos^2(\theta) = (1+\cos(2\theta))/2$, Equation (1.3) can be written as

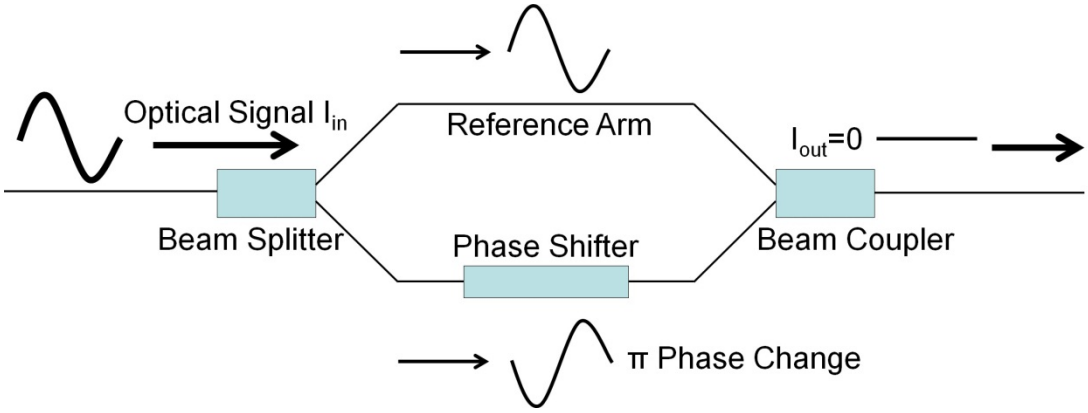
$$I_{out} = I_{in}\frac{1+\cos(\Delta\varphi)}{2} = \frac{I_{in}}{2} + \frac{I_{in}}{2}\cos(\Delta\varphi) \quad \textbf{(0.4)}$$

In Equation (1.4), the relation between the phase change and the output light intensity has been established. The intensity of the output light I_{out} of MZI has a cosine-dependence on the phase change Δφ. According to Equation (1.4), when there is no phase change Δφ=0, the output intensity equals the input intensity, $I_{out}=I_{in}$. When a π phase change is produced by the phase shifter, the output intensity equals 0, which is $I_{out}=0$. The above discussion does not take optical losses in the MZI structure into account, which lowers the extinction ratio. Fig.1.3 shows the typical phase-intensity modulation mechanism of an asymmetric MZI with a phase shifter in one arm.

As discussed, the key point of electro-optic modulator based on MZI then turns to the design of a phase shifter which can produce phase change modified by the applied electrical voltages.



(a) 0 phase change on phase shifter arm, $I_{out}=I_{in}$.



(b) π phase change on phase shifter arm, $I_{out}=0$.

Fig.1.3 Asymmetric MZI with phase shifter for phase-intensity modulation.

1.3 Phase shift mechanism

The phase shifter as a phase change generator together with the MZI structure turns phase change into intensity change. It is the key component of an electro-optic modulator to realise phase-intensity modulation. Varieties of phase shifters have been demonstrated [26-28, 42-45]. There are two popular phase shifters based on silicon material, the MOS capacitor phase shifter [26] and the PN

junction phase shifter [42-44]. The main difference between them is the method to change the density of free carriers, but the fundamental theory for both of them is the same, i.e. the free carrier plasma dispersion effect.

1.3.1 Free carrier plasma dispersion effect

The phase shift mechanism mostly used in silicon electro-optic modulators are the thermal-optic effect and the free carrier plasma dispersion effect (FCPDE), as the coefficients of other electro-optic effects in silicon are too weak to be used in practice [51]. The thermo-optic effect can only work in low frequency applications [8]. Therefore, the free carrier plasma effect is the choice for high speed modulation in silicon.

According to the classical dispersion theory (Drude model), in doped silicon, light of wavelength longer than the plasma wavelength is reflected and also light of wavelength smaller than the plasma wavelength is transmitted. The plasma wavelength is determined by the free carrier concentration in silicon, which is given as [100]

$$\lambda = 2\pi c\sqrt{\frac{\varepsilon_0 m}{Ne^2}} \qquad \textbf{(0.5)}$$

where c is the light speed in vacuum (3×10^8 m/s), ε_0 is the permittivity of free space (8.85×10^{-12} F/m), e is the electronic charge (1.6×10^{-19} C), m is the effective carrier mass (8.93×10^{-31} kg) and N is the carrier density. According to Equation (1.5), silicon

with lower doping concentration has a longer plasma wavelength. The plasma wavelength of silicon with a doping concentration of 1×10^{18} cm^{-3} (≈carrier concentration at room temperature) is 33 um. Therefore, when silicon doping concentration is lower than 1×10^{18} cm^{-3}, the communication wavelength 1.55 um is much smaller than the plasma wavelength.

In crystalline silicon material, there is no linear electro-optic (Pockels) coefficient and a very weak Franz-Keldysh effect [52]. Due to this fact, in high speed operation, the refractive index of silicon material is mainly affected by injection or depletion of free carriers in silicon. In this case, the refractive index change due to the thermo-optic effect is considered as background noise, as it could not respond to high frequency operations. Therefore, in doped silicon, a change of free carrier density ΔN results in a change of refractive index Δn and a change of free carrier absorption coefficient Δα.

The refractive index increases when carriers are removed or depleted from silicon; conversely, the refractive index decreases when free carriers are injected. This relation is described by the Drude-Lorenz equations that relate the change in the density of electrons (ΔN_e) and holes (ΔN_h) to the absorption coefficient (Δα) and refractive index change (Δn) [16]:

$$\Delta n = -(e^2\lambda^2 / 8\pi^2 c^2 \varepsilon_0 n)[\Delta N_e / m_{ce}^* + \Delta N_h / m_{ch}^*] \quad \textbf{(0.6)}$$

$$\Delta \alpha = (e^2\lambda^2 / 4\pi^2 c^3 \varepsilon_0 n)[\Delta N_e / m_{ce}^{*2}\mu_e + \Delta N_h / m_{ch}^{*2}\mu_h] \quad \textbf{(0.7)}$$

where e is the electronic charge, ε_0 is the permittivity of free space, n is the refractive index of unperturbed Si, ΔN_e is the electron density, ΔN_h is the hole

density, m_{ce}^{*} is the conductivity effective mass of electrons, m_{ch}^{*} is the conductivity effective mass of holes, μ_e is the electron mobility, and μ_h is the hole mobility.

It should be noted that generally speaking, free holes are more effective in changing the refractive index than free electrons [16]. At the wavelength of 1.55 μm, the refractive index and absorption coefficient change due to the change of electrons and holes, which were obtained from experimental absorption spectra through Kramers-Kronig analysis [15], are given by:

$$\Delta n_e = -8.8 \times 10^{-22} \Delta N_e \quad \textbf{(0.8)}$$

$$\Delta n_h = -8.5 \times 10^{-18} (\Delta N_h)^{0.8} \quad \textbf{(0.9)}$$

$$\Delta \alpha_e = 8.5 \times 10^{-18} \Delta N_e \quad \textbf{(0.10)}$$

$$\Delta \alpha_h = 6 \times 10^{-18} \Delta N_h \quad \textbf{(0.11)}$$

where electron and hole density changes are in units of cm^{-3}, Δn_e and Δn_h are the refractive index change caused by free electrons and holes, respectively; $\Delta\alpha_e$ and $\Delta\alpha_h$ are the absorption coefficient change caused by free electrons and holes, respectively. According to Equation (1.8) and (1.9), when the electron density change equals the hole density change, the refractive index change due to the electron density change is smaller than that due to hole density change (see Fig.1.4).

In other words, to have a better electro-optic modulation efficiency, the phase shifter should be fabricated on p-type doped silicon where holes are the majority carriers. For example, taking the same doping concentration of 5×10^{17} cm^{-3}

for both p-type and n-type silicon, the absolute value of refractive index change due to the electron and hole density change can be calculated as 4.4×10^{-4} and 1.2×10^{-3}, respectively.

The next issue is how to change the carrier density with voltage. The task in designing a silicon phase shifter is to find a structure where the carrier density in silicon waveguide is modulated by an applied voltage.

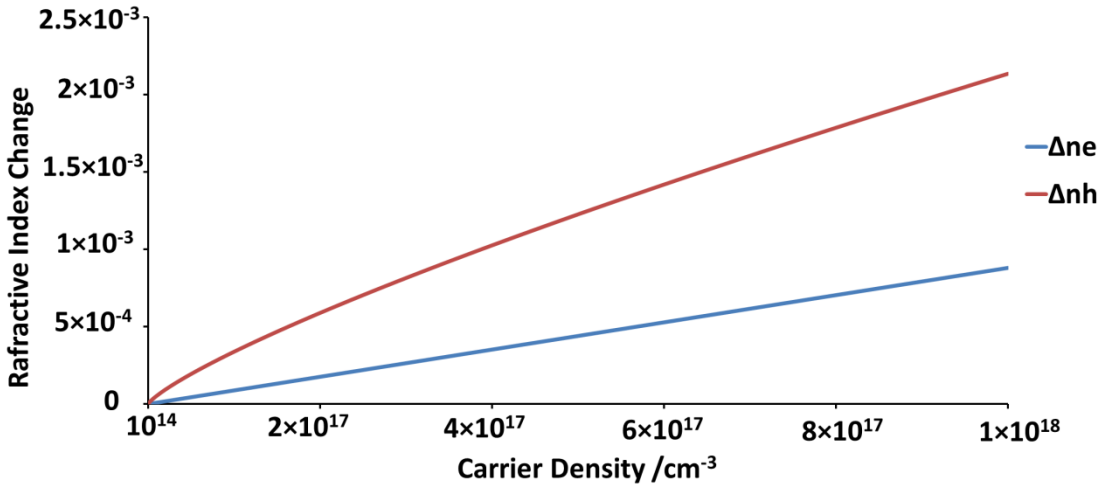


Fig.1.4 Carrier density – refractive index change (absolute value) relation (free carrier plasma effect). Δne and Δnh are the refractive index change due to electron and hole density change respectively. The curves are obtained by calculating Equation (1.8) and (1.9).

The change of the refractive index caused by the phase shift Δφ of the optical mode is given as [26]

$$\Delta\varphi = \frac{2\pi}{\lambda}\Delta n_{eff} L \qquad \textbf{(0.12)}$$

where L is the active length of the phase shifter, λ is the wavelength in free space, and Δn_{eff} is the effective refractive index change in the waveguide, which is introduced by the free carrier concentration change.

From Equation (1.12), the phase change made by the phase shifter can also be written as

$$\Delta\varphi = \Delta\beta \times L \tag{0.13}$$

where $\Delta\beta=2\pi\Delta n_{eff}/\lambda$ is the phase change per unit length generated by the active phase shifting length of the phase shifter.

As per Equation (1.13), the phase change Δφ is a function of the phase shifting length L which is also the active length of phase shifter. In order to achieve complete phase-intensity modulation, a π phase change is needed [49]. Therefore, the phase shift per unit length Δβ determines the total length of the phase shifter. Considering the relations of the carrier density change and the refractive index change, the strong effect of electrically modulated carrier density change is the key factor to make the device small. Thus, in the phase shifter design, it is also important to make the effect of carrier density changed by voltage as strong as possible.

Obviously, a good phase shifter achieves a π phase change with a small voltage and a short length. Therefore, the product of $V_\pi L$ can be used to describe the performance of phase shifter, where V_π is the voltage to achieve π phase change and L is the active length of the phase shifter. For example, $V_\pi L$ of the first silicon electro-optic modulator announced by Intel is 8 Vcm at maximum working speed of 1 GHz

[26]. And the later reported silicon modulator based on reverse biased PN junction also from Intel has a $V_\pi L$ value of 4 Vcm [42].

1.3.2 MOS capacitor phase shifter

A MOS capacitor is a well-known and widely used semiconductor device. By modifying the amount of carriers in the semiconductor, a MOS capacitor stores the electric charge [53]. Therefore, it can be used in a phase shifter as a carrier density controlling component. A typical n-type silicon MOS Capacitor is shown in Fig.1.5.

There are four working modes in a MOS capacitor referring to the free carrier distribution (see Fig.1.5), i.e. zero bias, accumulation, depletion and inversion, depending on the voltage bias [54]. In n-type silicon MOS capacitor, the free carriers are mainly electrons. When no bias is applied ($V_G=V_B=0$), the carriers are in thermal equilibrium and the electron concentration is roughly the doping concentration. When $V_G>V_B$ and $V_G>0$, the positive voltage attracts electrons to the oxide-silicon interface. The capacitor is in accumulation mode. The carrier concentration near the oxide-silicon interface is larger than the doping density depending on the applied voltage. When $V_G<V_B$ and $V_G<0$, the negative voltage pushes the electrons away from the oxide-silicon interface. Then the depletion region forms just below the oxide-silicon interface. The free carriers are in depletion mode, in which case the carrier concentration in depletion region is much lower than the doping concentration and is close to zero. With V_G continually reducing, the depletion region becomes larger and larger. However, when $V_G<<V_B$ and $V_G<0$, the depletion region width no longer increases, as a thin layer of holes appears near the oxide-

silicon interface to balance the potential in the silicon. Since holes are the minority carriers in n-type silicon, this layer is called the inversion layer. As a result, compared with the depletion mode, the carrier density near the oxide-silicon interface becomes slightly larger in the inversion condition.

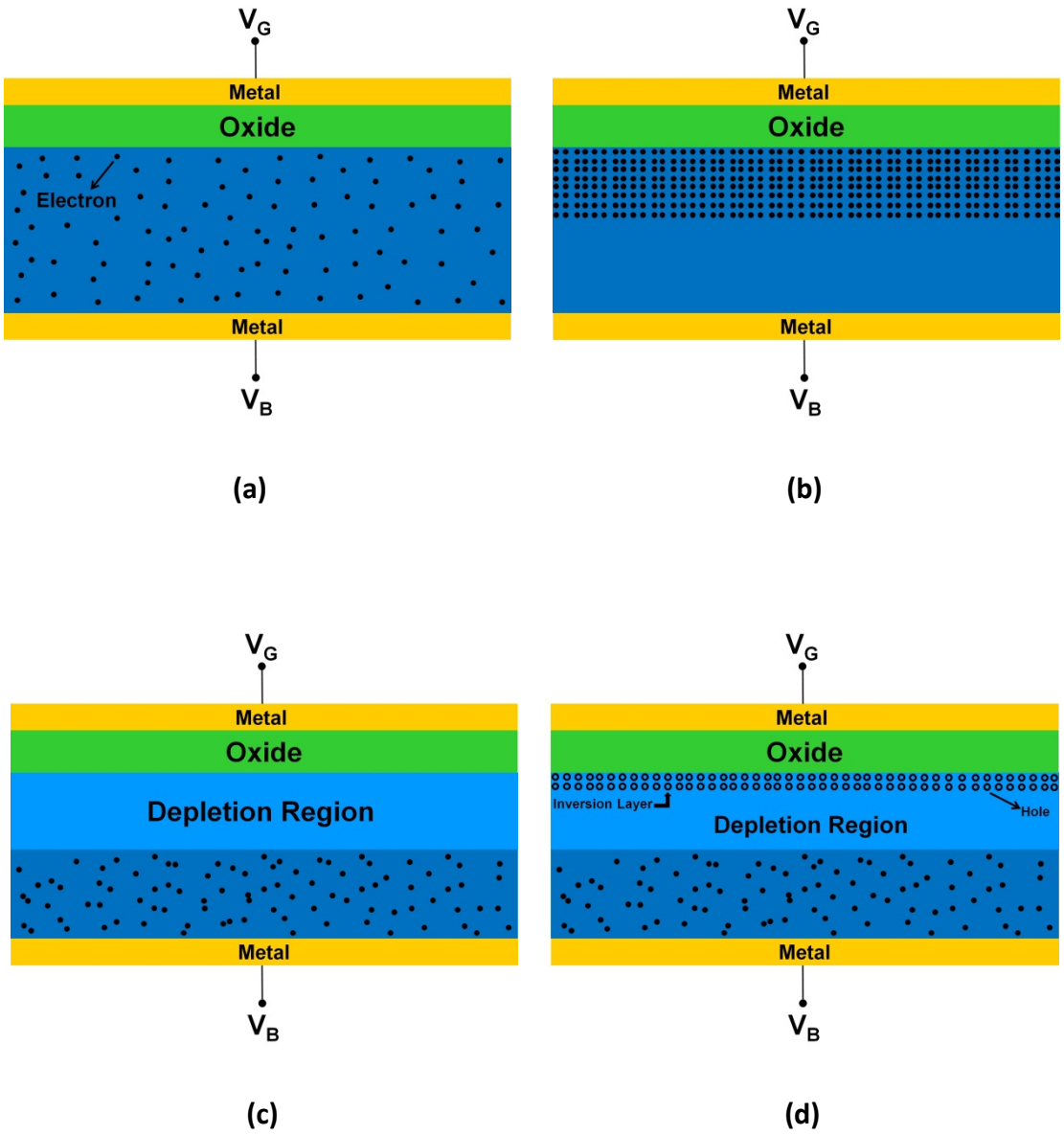


Fig.1.5 Free carriers in MOS capacitor (n-type substrate) under equilibrium, accumulation, depletion and inversion conditions. (a) Zero bias mode: V_G=V_B=0. Free carriers distribute evenly. (b) Accumulation mode: V_G>V_B, V_G>0. Free carriers

accumulate at the oxide-Si interface. (c) Depletion mode: $V_G<V_B$, $V_G<0$. Free carriers are depleted from the oxide-Si interface. (d) Inversion mode: $V_G<<V_B$, $V_G<0$. Minority carriers occur at the oxide-Si interface.

By controlling the V_{GB}, the carrier concentration in silicon substrate is changed by the applied voltage. Therefore, the refractive index is modulated by the applied voltage V_{GB}, according to the free carrier plasma effect.

1.3.3 PN junction phase shifter

A PN junction phase shifter uses a PN junction to control the carrier concentration change. A PN junction has two working modes, forward biased and reverse biased. The forward biased PN junction injects carriers into the junction region and decreases the depletion region width. However, when the PN junction is reverse biased, the free carriers are depleted in the junction and then the depletion region is enlarged.

It is suggested that in the carrier injection mode, the switch-off time is limited by minority carrier lifetime which is in the order of nanoseconds for typical silicon waveguides [27]. However, because carriers can be swept out more quickly than their recombination time, devices working in depletion mode can respond in a much shorter time, on the picosecond time scale [28]. Moreover, according to the investigation of III-V semiconductors optical modulators based on free carrier plasma effects, the limitation of modulation speed for a reverse biased PN junction phase shifter is the resistance–capacitance (RC) constant [55,56]. Therefore, PN junctions

working in reverse biased mode are better for high speed modulation, compared to forward biased PN junctions. Considering hole density change is more efficient than electron's in phase modulation, doping concentration in the p region should be lower than that in the n region to have larger phase change. In reverse biased PN junctions, the depletion layer mainly appears in the p region where holes are majority carriers, if the doping concentration in the n region is much higher than that in the p region. When a reverse bias is applied to a uniformly doped PN junction, the depletion layer width in the n region and the p region is given by [53]

$$W_n = \left\{ \frac{2\varepsilon_s (V_{bi} + V_a)}{e} [\frac{N_A}{N_D}][\frac{1}{N_A + N_D}] \right\}^{\frac{1}{2}} \quad \textbf{(0.14)}$$

$$W_p = \left\{ \frac{2\varepsilon_s (V_{bi} + V_a)}{e} [\frac{N_D}{N_A}][\frac{1}{N_A + N_D}] \right\}^{\frac{1}{2}} \quad \textbf{(0.15)}$$

$$W_d = W_n + W_p \quad \textbf{(0.16)}$$

where W_n is the depletion layer width in n-type region, W_p is the depletion layer width in p-type region, W_d is the total depletion layer width, N_A is the doping concentration of p-type dopant, N_D is the doping concentration of n-type dopant, ε_s is the semiconductor permittivity, e is the electronic charge, V_a is the applied voltage, and V_{bi} is the built-in voltage which is given as

$$V_{bi} = V_t \ln(\frac{N_A N_D}{n_i^2}) \quad \textbf{(0.17)}$$

where V_t=0.0259 V is the thermal voltage at room temperature (300 K) and n_i=1.5×10^{10} cm^{-3} is the intrinsic carrier concentration of silicon at 300 K. A typical value of the built-in voltage V_{bi} at room temperature with the donor concentration N_D of 5×10^{15} cm^{-3} and the accepter concentration N_A of 5×10^{16} cm^{-3} is 0.718 V.

The equilibrium condition of a PN junction is given by [53]

$$N_A W_p = N_D W_n \tag{0.18}$$

If the doping concentration in the n region is much higher than that in the p region (N_D >> N_A), W_n becomes very small, according to Equation (1.18). Hence, Equation (1.16) can be written as $W_d \approx W_p$.

Fig.1.6 shows the schematic diagram of a PN junction phase shifter. The device is realised in silicon on insulator (SOI) and the doping density in the n region is much higher than that in the p region. Fig.1.7 shows how the depletion layer changes when the reverse biased voltage is applied. In reverse bias condition, with the applied voltage increasing, the depletion region becomes larger, especially in the p-type doped region. During this process, as the free carriers, both electrons and holes, are swept out from some regions which then become depleted, the free carrier density in these new depletion regions reduces to ~0. Hence, the carrier density is changed by the reverse biased voltage.

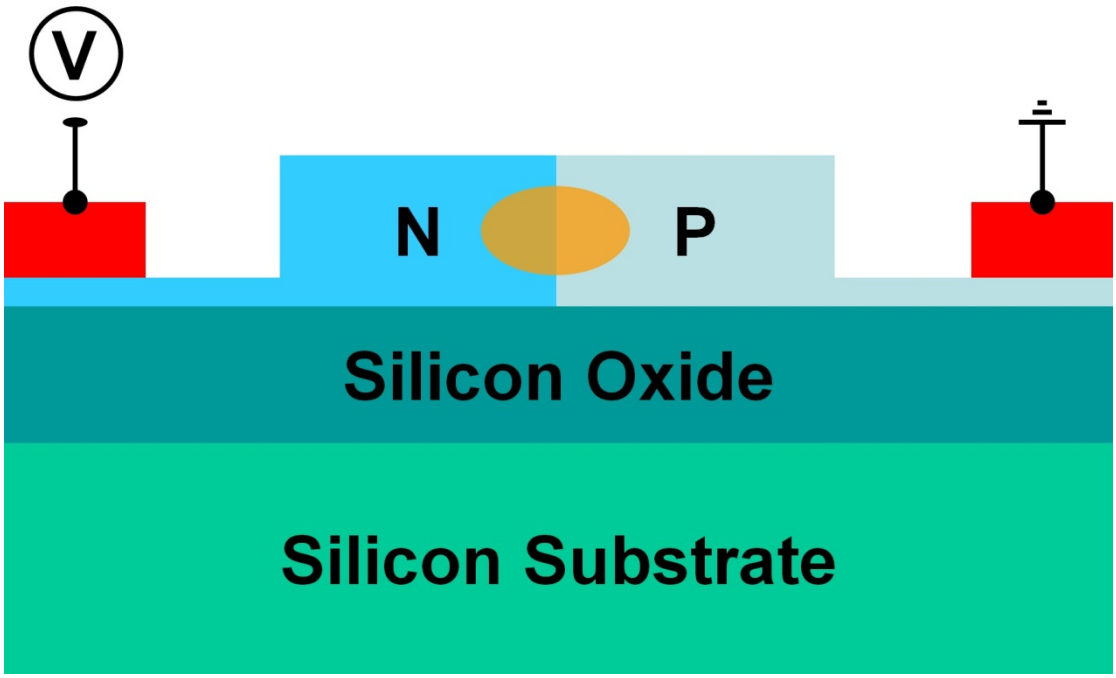
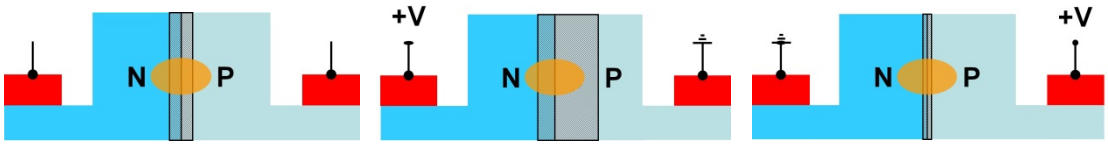


Fig.1.6 Schematic diagram of a PN phase shifter. The central top region is the silicon waveguide with PN junction situating in the middle. The orange region indicates the optical mode in the waveguide.



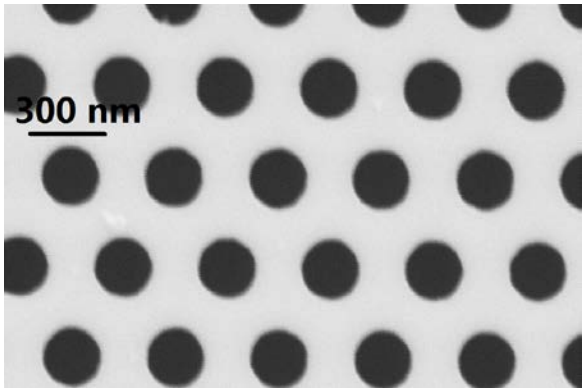
(a)0 Bias **(b)Reverse Bias** **(c)Forward Bias**

Fig.1.7 The depletion region change of a PN junction before and after applying the voltage (p-type doping concentration << n-type doping concentration). The shadow area is depletion region. The orange region is the optical mode. (a) Depletion region at 0 Bias; (b) Depletion region in reverse bias mode; (c) Depletion region in forward bias condition.

In forward bias mode, carriers are injected into the junction region and the depletion region is narrowed by the applied voltage. Therefore, some of the former depletion region becomes full of carriers. The carrier concentration in these regions increases from ~0 to the value corresponding to the doping density, or even higher. As a result, the carrier density is modified in the forward biased PN junction.

1.4 Slow light photonic crystal waveguide

Yablonovitch and John first proposed the concept of a photonic crystal (PhC) in 1987 [29,30]. Researchers all over the world have been attracted by the idea and thousands of papers have been published. A photonic crystal is a type of structure in which the refractive index varies periodically. In analogy with electrons in a periodic potential, forbidden bands can occur for electromagnetic waves in a periodic refractive index structure [31]. Therefore, photonic crystals exhibit photonic bandgaps in which light in a range of wavelengths cannot propagate [32]. 2D photonic crystals are periodic in two dimensions; correspondingly, 3D photonic crystals are periodic in all three dimensions (see Fig.1.8).



This illustration of 3D photonic crystals is unavailable due to copyright restrictions.

2D **3D**

Fig.1.8 2D and 3D [33] photonic crystals

By creating a line of defects as an optical path in photonic crystals, photonic crystal waveguides forms, where light can propagate [34]. Photonic crystal waveguides also exhibit a slow light propagation [35-37], which is due to the coherent backscattering mechanism [38] (see Fig.1.9). The forward propagating and coherently backscattered light forms a slowly moving interference pattern which can be considered as a slow mode with low group velocity.

Slow light is a promising technique for optical delay lines, all-optical buffers, and synthetic aperture radar applications. In contrast to resonant cavities that enable a similar resonant enhancement, photonic crystal waveguides offer large bandwidths which are critical for the processing of ultrashort optical signals [39].

This illustration of slow light mechanism in photonic crystal waveguides is unavailable due to copyright restrictions.

Fig.1.9 Illustration of slow light mechanism in photonic crystal waveguides, namely coherent backscattering [38]. "a" is the period of the photonic crystals.

The slow light property in photonic crystals is described by the slowdown factor which is defined as the ratio of the phase velocity over the group velocity, $S = v_\phi/v_g$. One of the most important reasons why slow light in photonic crystal waveguides is so attractive is that it enhances the interaction effects in a material, such as the free carrier dispersion effect in silicon. Slow light is really an amazing property for an electro-optic modulator based on a MZI structure, as thermo-optic and electro-optic interaction scale with the slowdown factor. For conventional MZI modulators based on silicon rib waveguides, a few millimetres long waveguides is typically required to achieve a π phase change. However, by using a slow light photonic crystal waveguide, the π phase shifting length can be reduced to ~10s of micrometres due to the slow light enhancement. Fig.1.10 shows that the phase change is enhanced by the slow light effect. The corresponding device length required to achieve a π phase shift, L_π, scales inversely as the slowdown factor, so $L_\pi(\text{slow})=L_\pi(\text{fast})/S$.

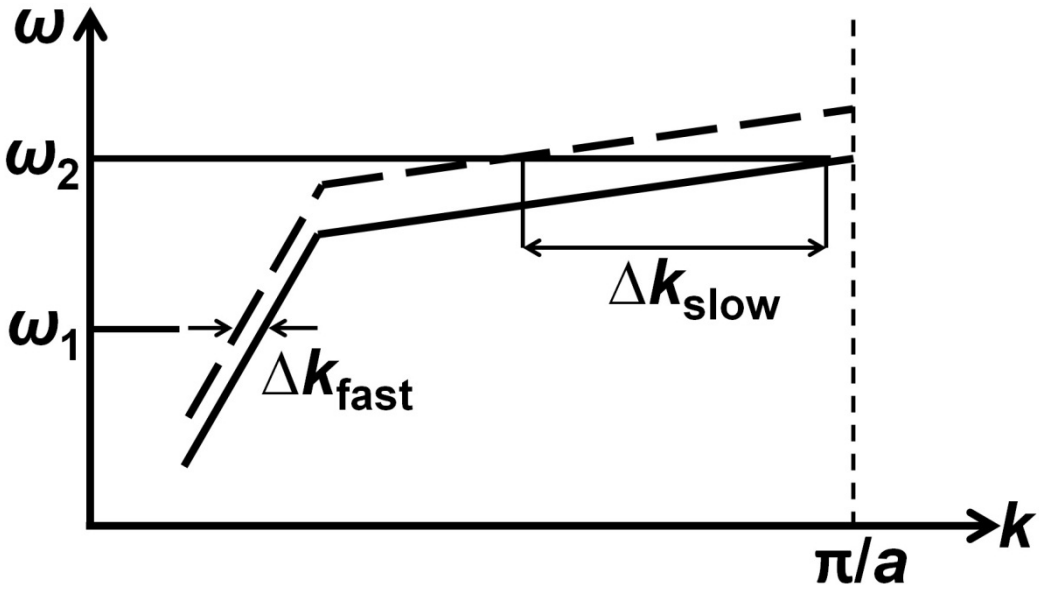


Fig.1.10 Dispersion (*ω*-*k*) diagram showing the slow light enhancement. For a given refractive index change Δn (from solid to dashed line), the phase change (proportional to Δ*k*) in the slow light regime is much larger than in the fast light regime.

Although slow light in photonic crystals appear promising, they have two disadvantages. The first one is the high dispersion. The typical operating point for slow light is on a near-parabolic dispersion curve near the edge of the Brillouin zone, which seriously limits the bandwidth due to large group velocity dispersion [40]. The other disadvantage is the trade-off between slowdown factor and bandwidth, as a high slowdown factor only occurs over a narrow range of wavelength. By using slow light photonic crystal waveguides, the device footprint can be reduced, but the bandwidth is limited as well.

However, researchers were able to demonstrate flat band slow light in photonic crystal waveguides [41]. The concept of slow light "dispersion engineered"

photonic crystal waveguides allows us to create waveguides with nearly constant group index of 32.5, 44 and 49 and a bandwidth of 14 nm, 11 nm and 9.5 nm, respectively (see Fig.1.11), which exemplifies the slow light enhancement possible with PhC waveguides.

This illustration of transmission spectra of slow light engineered photonic crystal waveguides is unavailable due to copyright restrictions.

Fig.1.11 Transmission spectra of slow light engineered photonic crystal waveguides. [41] The black solid lines show the measured transmission spectra. The blue and red solid lines show the experimental and calculated group index curves, respectively. The four figures are of different slow light PhC design and therefore, have different group index.

In summary, the slow light phenomenon allows us to reduce the phase length of the phase shifter leading to a reduction in the length of the electric-optic

modulator; the penalty for this enhancement is a reduced bandwidth, although very practical bandwidths exceeding 1 THz are possible.

1.5 Different types of silicon modulators

In this section, several different types of silicon electro-optic modulators are introduced. A silicon thermo-optic modulator based on slow light photonic crystal waveguides is also discussed, as a nice example to show how phase shifter length is reduced by slow light enhancement.

1.5.1 Modulator based on MOS capacitor

Ansheng Liu et al,. from Intel demonstrated the first 1 GHz silicon electro-optic modulator in 2004. This milestone work was based on the free carrier plasma dispersion effect in a silicon MOS capacitor (see Fig.1.12). A thin gate oxide layer (12 nm) is between the p-type poly-silicon as a transparent conducting layer with an active doping concentration of ~3×10^{16} cm^{-3} and the n-type silicon substrate with the active doping concentration of ~1.7×10^{16} cm^{-3}.

This illustration of a MOS capacitor waveguide phase shifter on SOI wafer is unavailable due to copyright restrictions.

Fig.1.12 Schematic diagram showing the cross-sectional view of a MOS capacitor waveguide phase shifter on SOI wafer [26]. p-Poly-Si is a transparent conducting layer to connect the metal contact to the silicon waveguide (n-Si). The silicon under the metal contacts is highly doped (1×10^{19} cm^{-3}) to reduce the contact resistance.

The device is working in the accumulation mode. During the accumulation operation, the n-type silicon in the phase shifter is grounded and a positive driving voltage V_D is applied to the p-type polysilicon. When a positive voltage V_D is applied to the device, a thin charge layer is accumulated on both sides of the gate oxide, which behaves very much like a capacitor. The voltage-induced charge density change ΔN_e (for electrons) and ΔN_h (for holes) is related to the driving voltage as [26]

$$\Delta N_e = \Delta N_h = \frac{\varepsilon_0 \varepsilon_r}{e t_{ox} t}[V_D - V_{FB}] \qquad \textbf{(0.19)}$$

where ε_0 and ε_r are the vacuum permittivity and low-frequency relative permittivity of the oxide, e is the electron charge, t_{ox} is the gate oxide thickness, t is the effective charge layer thickness, and V_{FB} is the flat band voltage of the MOS capacitor.

The modulator built with this phase shifter is based on an asymmetric MZI structure with an optical path length difference of ~16.7 um between the two arms. Several different phase shifter lengths have been tried, which is, L=1, 2.5, 5, 8 mm. The $V_\pi L$ product of the device is ~ 8 Vcm. As the phase shifter of this modulator is based on a MOS capacitor, the on-chip voltage has a high-frequency roll-off, which is governed by the output impedance of the driving circuitry and capacitance of the phase shifter [26]. Therefore, the modulation speed is limited by this effect, which is a disadvantage compared with other electro-optic modulators that are not based on a MOS capacitor structure. Also, the length of this modulator is in millimetres. By using slow light photonic crystal waveguides, both the length and consequently, the capacitance of the modulator can be reduced.

1.5.2 Modulator based on carrier depletion PN junction

The typical carrier depletion optical modulator uses reverse biased PN junctions to control the free carrier concentration. Ansheng, Liu et al,. from Intel demonstrated a modulator with 30 Gb/s modulation speed in 2007 [42]. Fig.1.13 is the cross-sectional view of the reversed biased PN phase shifter.

This illustration of a reverse biased PN phase shifter is unavailable due to copyright restrictions.

Fig.1.13 Cross-sectional view of a reverse biased PN phase shifter [42]. The "n++" and "p++" regions are to reduce the contact resistance. Traveling-wave electrodes allow electrical and optical signal co-propagation along the waveguide and therefore keep the RF attenuation low.

The modulator is based on an asymmetric MZI structure with the optical path difference of ~20 um. The modulator is fabricated on SOI. The p-type doping concentration is ~1.5×10^{17} cm^{-3} in the PN junction, and the n-type doping concentration varies from ~3×10^{18} cm^{-3} near the top of the cap layer to ~1.5×10^{17} cm^{-3} at the PN junction. Thus, the n-type doping concentration is much higher than the p-type doping concentration, which leads to the depletion layer formation mainly in the p region. According to the free carrier plasma effect, high phase shifting efficiency can be achieved by this design. The $V_{\pi}L$ product for the device is ~ 4 Vcm, which is only half of that of the modulator based on MOS capacitor [55]. The 3dB band width of this modulator is over 20 GHz.

The phase shifting length of this modulator is still relatively long, i.e. between 1 mm to 5 mm. By applying slow light enhancement, the phase shifter length could be reduced. As a result, the capacitance can be lowered and higher modulation speed can be achieved.

1.5.3 Modulator based on forward biased PIN junction

This silicon electro-optic modulator is based on a forward biased PIN junction with PhC waveguides in the MZI arms. As the light in PhC waveguides has slow group velocity, the interaction length of phase shifting can be reduced [43]. The PIN junction is in one arm with PhC waveguide in the i region and p, n regions on the two sides (see Fig.1.14).

As the group velocity of light in the PhC waveguides is designed as 0.1 of the light speed in vacuum, PhC waveguides provide 10 times the enhancement. Hence, the active phase shifting length is only 1/10 of the conventional phase shifter, which is 80 um long. The “on” and “off” voltage to drive the phase shifter are 2 V and -1 V, respectively. As a result, the $V_{\pi}L$ product of the phase shifter is 0.024 Vcm. The total length of the MZI modulator is 1 mm. The maximum modulation speed is 1 Gbit/s [44].

In this design, a forward biased PIN junction generates current and consequently heat in the waveguide region. Hence, the thermal-optic effect is produced and acts as noise, which lowers the extinction ratio. Moreover, compared with the MOS capacitor working in depletion mode, the forward biased PIN junction

has a lower modulation speed.

This illustration of a PIN phase shifter with silicon photonic crystal waveguide is unavailable due to copyright restrictions.

Fig.1.14 PIN phase shifter with silicon photonic crystal waveguide [44]. The two PhC waveguides are the two arms of a symmetric MZI modulator. Both of the PhC waveguide are 80 um long. The PIN junction phase shifter is in the right arm.

1.5.4 Modulator based on micro-ring resonator

The first silicon electro-optic modulator based on micro-ring resonator which is different from MZI as modulation structure was demonstrated in 2005 [45]. This modulator uses a forward biased PIN junction which has been proven to have high modulation efficiency [45], to electrically modulate the refractive index change. The ring resonator is a light-confining resonating structure, which can enhance the

refractive index change effect. Therefore, by using micro-ring resonator structure, the size of the modulator is reduced to only 12 um in diameter (see Fig.1.15).

This illustration of micro-ring resonant electro-optic modulator is unavailable due to copyright restrictions.

Fig.1.15 Micro-ring resonant electro-optic modulator [45]. A PIN junction is used to inject carriers into the ring waveguide and operate the refractive index. Consequently, the transmission in the strip waveguide is modulated by shifting the operating wavelength of the ring resonator.

The resonance wavelength is sensitive to the effective index of the ring waveguide. Therefore, by tuning the effective index of the ring waveguide, the light transmission in the strip waveguide is strongly modulated. The PIN junction is used to electrically modify the effective index. The ring waveguide is in the i region. The p^+ region is inside the ring while the n^+ region is around the ring waveguide. The driving voltage is 6.9 V (peak to peak) at the modulation speed of 1.5 Gbit/s [45]. As the bandwidth of the ring resonator is small, the modulator has a very small optical bandwidth (less than 0.1 nm around the centre wavelength).

1.5.5 Thermo-optic modulator with slow light PhC waveguides

By using the slow light effect in PhC waveguides, this silicon thermo-optic modulator which is based on a symmetric MZI has a relatively short phase shifter (Fig.1.16). A π phase shift was achieved in only 80 um long PhC phase shifter [57].

The phase shift mechanism is the thermo-optic effect. In silicon, the refractive index increases with temperature. The temperature is controlled by an integrated nickel microheater placed on the PhC phase shifter. The total phase change is ΔkL where Δk is the k-vector changed by the thermo-optic effect and L is the phase shifting length. When heat is applied, the wave vector shift is given by $\Delta k = \Delta n \omega_0 S$, where Δn is the refractive index change, ω_0 is the frequency and S is the slowdown factor. The slowdown factor S is defined as $S=n_g/n$, where n_g is the group index and n is the phase index. As a π phase shift is required for phase-intensity modulation $\Delta kL=\pi$, therefore, the phase shifting length L is reduced by the slow light enhancement. The group index of the PhC waveguides was designed to be 28. And the bandwidth of this modulator is 11 nm.

Although the modulation speed (~50 KHz) is limited by the slow response of the thermo-optic effect, this design shows that the phase shifter length is reduced by slow light effect. By using slow light PhC waveguides, both short length and high modulation speed can be achieved in silicon electro-optic modulator based on a MOS capacitor phase shifter working in depletion mode.

This illustration of thermo-optic modulator with slow light PhC waveguides is unavailable due to copyright restrictions.

Fig.1.16 Thermo-optic modulator with slow light PhC waveguides [57]. (a) Microscope view of the whole device showing the nickel microheater used to change the . The 80 um long PhC waveguides are in the both arms of MZI modulator. (b) SEM picture of the cross section of the flowable oxide (FOx) clad PhC. FOx is a type of spin-on-glass. (b) is the cross-sectional view of (c). The bright rectangles are the silicon layer and the gaps between them are photonic crystal holes. The holes are filled with FOx. (c) Closeup of the slow light engineered PhC waveguide. The first and second rows are laterally shifted. (d) SEM picture of the overview of the MZI structure (prior to FOx cladding and contact deposition).

1.6 Summary & layout of this thesis

As on-chip data links with large bandwidth and high speed have become more and more important, silicon electro-optic modulators as the key component in this system has been widely studied in the past few years. In summary, all these silicon electro-optic modulators are based on the free carrier plasma dispersion effect. Modulation speed, bandwidth, power consumption and device footprint are the major factors in the modulator study and design. New designs have been proposed continuously. New materials have been investigated and tested to use in the modulators. And new fabrication technology has been developed to improve performance of silicon electro-optic modulators. However, all these factors must be considered in a comprehensive way for the modulator design. For example, electrons move faster than holes [58], thus, in order to achieve high modulation speed, n-type silicon is better than p-type one to use in the modulator. Nevertheless, the refractive index change due to a certain hole density change is larger than that due to the same electron density change, in which case p-type silicon is better than n-type one. Therefore, it is critical to find a balance among all factors in the modulator design.

In this work, a MOS capacitor working in depletion mode was chosen as the phase shifter design, due to the following reasons. First of all, there is no heat generation in the phase shifter, as the device works in depletion mode and no current flows through the device. Secondly, carrier depletion is faster than carrier accumulation, which results in faster modulation speed. Thirdly, as the free carriers in the waveguide region are depleted, the optical loss due to free carrier absorption

is lower in this design than that in carrier accumulation designs. By using a slow light PhC waveguide, the phase shifter length could be reduced, which results in a smaller capacitance. Therefore, high speed modulation can be achieved.

This work describes the study and the fabrication of a new type of silicon electro-optic modulator based on the MZI structure with the slow light PhC waveguides. The project includes electrical and optical design, simulation, fabrication and testing. In chapter 2, phase shifter design issues are studied, in which electrical simulations are run to investigate the electrical performance of the phase shifter. In chapter 3, the electrical and optical properties of indium tin oxide (ITO) as a transparent conductor material are studied and tested. In chapter 4, the fabrication and optimisation of aluminium electrical contacts to silicon are investigated, in which the contact resistance is measured by the transmission line method (TLM). In chapter 5, the silicon electro-optic modulator and phase shifter are fabricated and tested. In chapter 6, problems as well as future work of the modulator and the phase shifter are discussed.

Chapter 2

Electrical Simulation & Design

Our electro-optic modulator is based on an asymmetric Mach-Zehnder interferometer (MZI) structure with the phase shifter in one arm. In order to realize electro-optic modulation, the MZI structure turns a phase change into an optical intensity change. Therefore, phase shifters are the key component of the device. The electrical simulation of the phase shifter is to model the electrical performance of its structure and material. Electrical design is to find the best solution with low RC constant (allowing high modulation speed) and large depletion region width (large carrier density change). In this chapter, a carrier depletion based MOS capacitor phase shifter is designed and its electrical properties are investigated by using a commercial electrical modelling tool – Synopsys TCAD.

2.1 Phase shifter design

The phase shifter is a MOS capacitor based on carrier depletion. Fig.2.1 shows the schematic diagram of the proposed phase shifter. N-type silicon is chosen to be the substrate for high speed modulation as discussed in the previous chapter. Applying a negative voltage to the central Al contact, the free carrier density in the waveguide region decreases, as carriers in this region has been depleted (see Fig.2.2). Operating in such way, refractive index of the silicon waveguide is modulated by the applied voltage. The optical signal travelling through the waveguide experiences a refractive index change. As a result, the phase of the optical signals changes at different voltages.

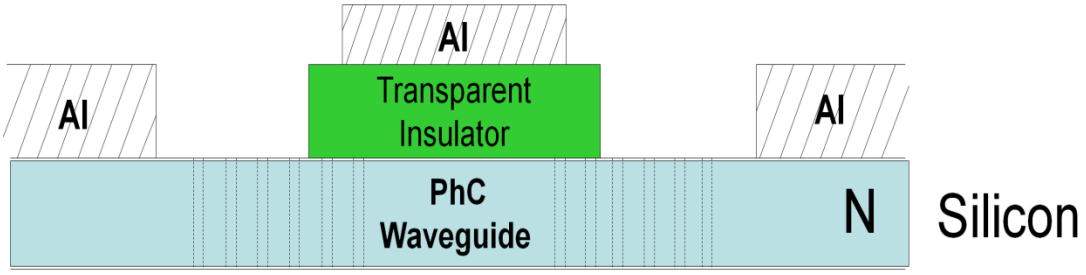


Fig.2.1 Schematic diagram of phase shifter with no voltage applied to Al contacts. The silicon substrate is n-type doped. The Al contacts are on the transparent insulator layer and silicon. The transparent insulator separates the Al contact from the silicon waveguide to reduce optical loss due to metal absorption.

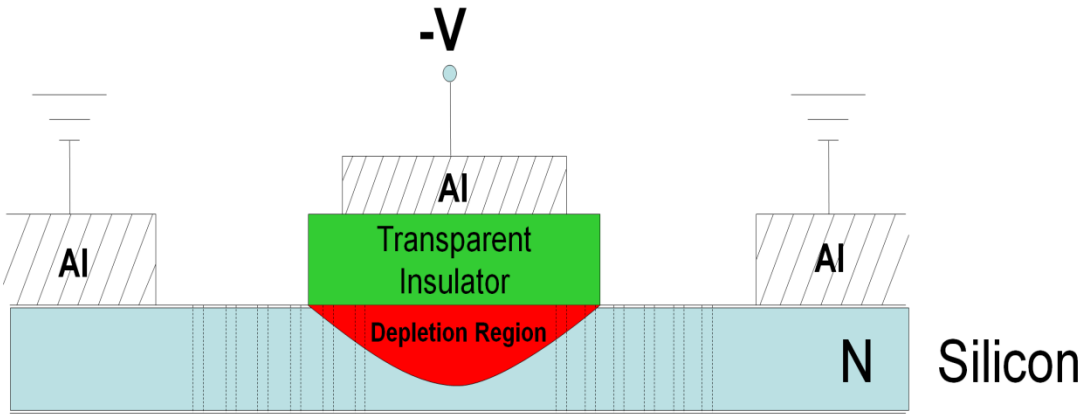


Fig.2.2 Schematic diagram of phase shifter with negative voltage applied to Al contacts. The silicon substrate is n-type doped. The Al contacts are on the transparent insulator layer and silicon. The transparent insulator separates the Al contact from the silicon waveguide to reduce the optical loss due to metal absorption. The red area is the depletion region.

The transparent insulator is a spacer between aluminium central contact and silicon waveguide to isolate optical modes from metal contacts, as metals such as aluminium causes significant absorption loss when they are directly placed on top of silicon waveguides [59]. In the MOS capacitor phase shifter, transparent insulator is also used as gate dielectric. However, to decide thickness of the transparent insulator is not easy. On one hand, the transparent insulator should not be too thick, as the voltage required to deplete the carriers in the waveguide scales with the thickness of the insulator. On the other hand, the absorption caused by aluminium metallisation increases when the insulator thickness reduces [60]. Besides, the transparent insulator also has great influence on the device RC constant which limits the working speed. Therefore, finding an ideal thickness of the insulator layer is very

important for the phase shifter. The equivalent circuit for the phase shifter is basically that of a MOS capacitor, and can easily be described analytically. The capacitance C'(depl) per unit area of the MOS capacitor in depletion mode is given as [53]

$$\frac{1}{C'(depl)} = \frac{1}{C_{ox}} + \frac{1}{C'_{SD}} \tag{2.1}$$

C_{ox} is the capacitance of the gate oxide (insulator) and, C'_{SD} is the capacitance of the depletion region.

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.2}$$

$$C'_{SD} = \frac{\varepsilon_s}{t_d} \tag{2.3}$$

where ε_{ox} is the permittivity of the transparent insulator, ε_s is the permittivity of silicon, t_{ox} is the thickness of the transparent insulator, t_d is the depletion region width. Considering Equation (2.2) and (2.3), Equation (2.1) can be written as

$$C'(depl) = \frac{\varepsilon_{ox}}{t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_s} t_d} \tag{2.4}$$

Assuming the phase shifter is working in depletion mode with the maximum depletion region width, which gives the largest carrier density change, C'_{SD} is only

determined by the doping level of the silicon substrate. The depletion region reaches its maximum width when the inversion layer which is a thin layer of minority carriers occurs at the insulator-semiconductor interface. Once the doping level of the silicon substrate is fixed, according to Equation (2.4), the capacitance C'(depl) is a function of the permittivity of the transparent insulator material and its thickness. The total capacitance of the MOS capacitor can then be written as

$$C = S \times C'(delp) = \frac{S\varepsilon_{ox}}{t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_s} t_d} \quad \textbf{(2.5)}$$

where S is the area of the MOS capacitor.

The maximum depletion region width t_{dT} can be written as [53]

$$t_{dT} = \left(\frac{4\varepsilon_s \phi_{fn}}{eN_d}\right)^{1/2} \quad \textbf{(2.6)}$$

with $e=1.6\times10^{-19}$ C the electronic charge. The potential ϕ_{fn} is the difference between the intrinsic Fermi energy E_{Fi} and Fermi energy E_F, which is given by

$$\phi_{fn} = V_t \ln\left(\frac{N_d}{n_i}\right) \quad \textbf{(2.7)}$$

where $V_t=0.0259$ V is the thermal voltage at 300 K, N_d is the donor doping concentration and $n_i=1.5\times10^{10}$ cm^{-3} is the intrinsic carrier concentration in silicon at

300 K, ε_s=1.04×10^{-12} F/cm is the permittivity of silicon. A typical value of ϕ_{fn} for a doping concentration of 1×10^{17} cm^{-3} is 0.407 Volts.

The silicon layer of silicon-on-insulator (SOI) wafer used in this work is 220 nm thick. The effective refractive index change is obtained by converting the change of carrier concentration into a refractive index change via the plasma effect. At the meantime, the overlap between the optical mode and the carrier density changing region must be taken into account. As a simple approximation, by assuming carrier concentration in the depletion region is zero and that outside the depletion region equals the doping concentration, the effective refractive index change Δn_{eff} is given as

$$\Delta n_{eff} = \frac{t_{dT}}{t_{si}} \Delta n \tag{2.8}$$

where t_{si} is the thickness of the silicon layer. In n-type silicon, the total free carrier density change is mainly the electron density change, $\Delta N \approx \Delta N_e$. And also in full depletion condition, the electron density change in MOS capacitor equals the n-type doping concentration, $\Delta N_e \approx N_d$. Therefore, combining with Equation (1.7), Equation (2.8) can be written as

$$\Delta n_{eff} = -8.8 \times 10^{-22} \frac{t_{dT}}{t_{si}} N_d \tag{2.9}$$

By calculating Equation (2.6) and (2.9) which are both functions of doping concentration, the maximum depletion region width and effective refractive index change at a certain doping concentration is obtained (see Fig.2.3). The t_{dT} curve

shows that the depletion region width scales inversely with doping concentration. The Δn_{eff} curve shows the effective refractive index change due to electron density change. Fig.2.3 shows that with increasing the doping density, the maximum depletion region width decreases, while the effective refractive index change increases.

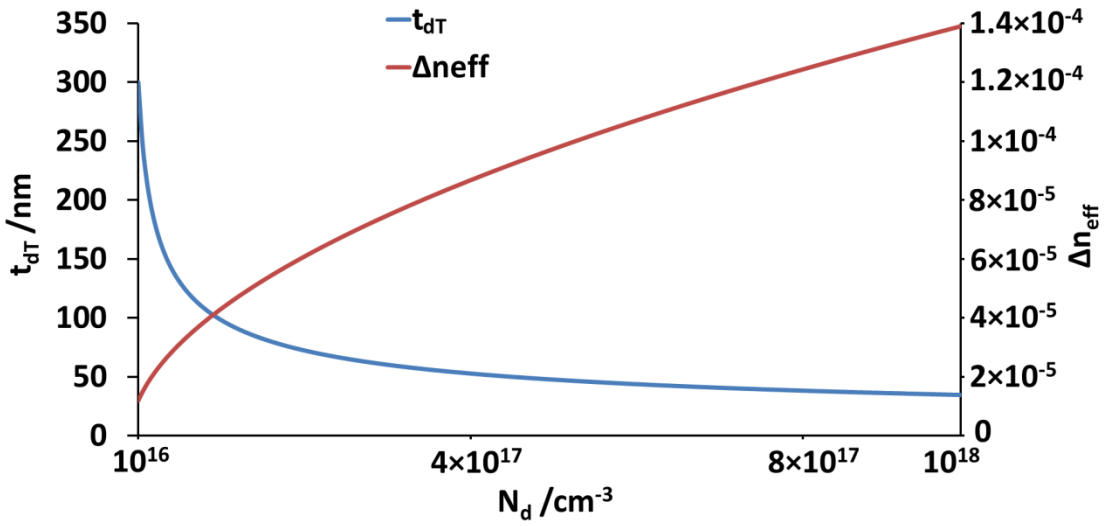


Fig.2.3 Maximum depletion region width (t_{dT}) and effective refractive index change due to electron density change (Δn_{eff}) in MOS capacitor working in depletion mode with different doping concentrations (N_d). The t_{dT} curve is generated by calculating Equation (2.6) and (2.7), assuming the insulator layer thickness is zero. The Δn_{eff} curve is produced by calculating Equation (2.9). In n-type silicon, the electron density is roughly the n-type doping density, $\Delta N_e \approx N_d$.

Ideally, it is better to have the entire silicon layer depleted by the applied voltage. As a result, the optical mode in silicon waveguide experiences the same refractive index change. Otherwise, the non-uniform refractive index changes the mode profile and causes dispersion [61]. In terms of getting uniform refractive index

change in the waveguide region, it is better to choose lightly doped silicon whose maximum depletion region width is at least 220 nm. Nevertheless, lower doping concentration means a smaller carrier density change. Then, the refractive index change becomes smaller and the light travelling in the waveguide has a smaller phase change. Although the phase change per unit length is smaller in this case, it could be compensated by increasing the phase shifter length to achieve π phase change for modulation. However, long phase shifter length also increases propagation loss. On the other hand, with increasing doping concentration, the carrier density change becomes larger. But the optical loss becomes higher due to the carrier absorption. At the same time, the mode profile and the dispersion are getting worse. For example, the maximum depletion region width of n-type silicon with doping concentration of 1×10^{19} cm^{-3} is only 11.67 nm by calculating Equation (2.6) and (2.7), while the absorption coefficient can be as high as 369.2 dB/cm [28]. The maximum depletion region width of n-type silicon with doping concentration of 4×10^{17} cm^{-3} is 53.54 nm, while the absorption coefficient is only 14.8 dB/cm. The free carrier absorption loss in decibels α_π on the π phase shifting length is given by [61]

$$\alpha_\pi = 10\log(e^{-\Delta\alpha L_\pi}) \tag{2.10}$$

where Δα is the free carrier absorption loss and L_π is the π phase shifting length which can be obtained from Equation (1.11).

In n-type silicon, the change of free carrier absorption coefficient is mainly because of the change of free electron concentration, $\Delta\alpha\approx\Delta\alpha_e$. Therefore, combining with Equation (1.10), Equation (2.10) can be written as

$$\alpha_\pi = 10\log(e^{-8.5\times10^{-18}\Delta N_e L_\pi}) \quad \textbf{(2.11)}$$

Equation (2.11) shows that α_π is a function of ΔN_e and L_π. And according to Equation (1.11), L_π is a function of $\Delta\varphi$, λ and Δn_{eff}. Therefore, at a given wavelength λ=1.55 um and with a given phase change $\Delta\varphi=\pi$, L_π is determined by Δn_{eff}. According to Equation (2.9), Δn_{eff} is a function of t_{dT} and ΔN_e. And t_{dT} is determined by N_d (Equation (2.6) and (2.7)). Also in an n-type silicon MOS capacitor working in depletion mode, the free electron density change equals the doping concentration, $\Delta N_e=N_d$. Thus, α_π is ultimately determined by N_d. Combining Equation (1.11), (2.6), (2.7), (2.9) and (2.11), α_π in n-type silicon MOS capacitor working in depletion mode can be written as

$$\alpha_\pi = 10\log\{\exp[-2.41\times10^3\lambda t_{si}(\frac{\varepsilon_s V_t}{eN_d}\ln(\frac{N_d}{n_i}))^{-\frac{1}{2}}]\} \quad \textbf{(2.12)}$$

The relation between the free carrier absorption loss α_π on the π phase shifting length and doping concentration N_d is shown in Fig.2.4. It is easy to find that the absorption loss increases with the doping concentration. Here, we mainly consider the absorption loss in zero phase shift situation, in which case output from the MZI modulator is 1. In the π phase shift situation, the depletion region occurs in the phase shifter waveguide and the optical loss due to the free carrier absorption reduces. The loss change between the “0” state and “1” state in the phase shifter arm lowers the extinction ratio of the MZI modulator. The decrease in loss only happens in the phase shifter arm which means the output light from the MZI modulator cannot entirely cancel in the “0” output state. The extinction ratio of the

MZI modulator is $I_o/\Delta\alpha_0$, where I_o is the output of the MZI modulator in the "1" state and $\Delta\alpha_0$ is the loss change in the phase shifter arm between the "1" and "0" state of the modulator. The output I_o changes conversely with the doping concentration and the loss change $\Delta\alpha_0$ increases with the doping concentration. Thus, it is easy to find that the extinction ratio decreases when the doping concentration increases.

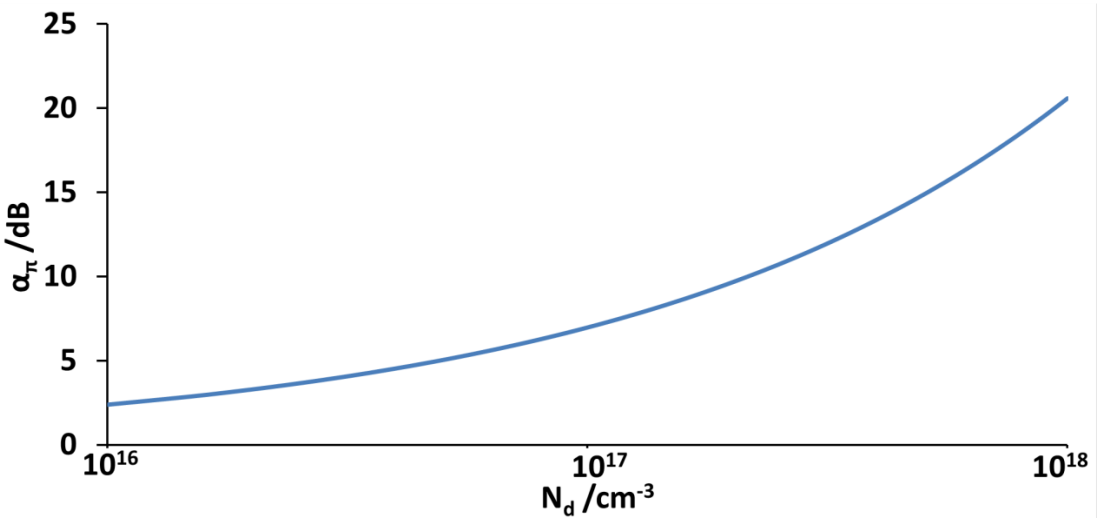


Fig.2.4 α_π Vs N_d in n-type silicon phase shifter based on a MOS capacitor working in depletion mode. wavelength λ=1.55 um. silicon thickness t_{si}=220 nm. The curve is obtained by calculate Equation (2.12).

Moreover, it is easier to deplete low doped silicon, as the voltage required to achieve this operation is low. Nevertheless, highly doped silicon needs larger voltage to get carriers fully depleted which means higher power consumption. The theoretical analysis for n-type silicon as phase shifter substrate with some typical doping concentrations is shown in Table 2.1.

N_d /cm^{-3}	t_{dT} /nm	Δn	$Δn_{eff}$	$L_π$ /mm	Δα /cm^{-1}	$α_π$ /dB
10^{16}	299	$8.8×10^{-6}$	$8.8×10^{-6}$	88.068	0.085	3.25
$5×10^{16}$	141.9	$4.4×10^{-5}$	$2.84×10^{-5}$	27.305	0.43	5.04
$1×10^{17}$	102.6	$8.8×10^{-5}$	$4.11×10^{-5}$	18.877	0.85	6.97
$3×10^{17}$	61.3	$2.64×10^{-4}$	$7.36×10^{-5}$	10.537	2.55	11.67
$5×10^{17}$	48.2	$4.4×10^{-4}$	$9.64×10^{-5}$	8.0403	4.25	14.84
$1×10^{18}$	34.8	$8.8×10^{-4}$	$1.39×10^{-4}$	5.5749	8.5	20.58
$5×10^{18}$	16.2	0.0044	$3.24×10^{-4}$	2.3888	42.5	44.09
$1×10^{19}$	11.7	0.0088	$4.67×10^{-4}$	1.66	85	61.28

Table 2.1 Theoretical analysis for typical doping concentrations of n-type silicon as phase shifter substrate. Max depletion region width (t_{dT}) is calculated by Equation (2.6) and (2.7). Refractive index change (Δn) is calculated by Equation (1.7). Effective refractive index change ($Δn_{eff}$) is calculated by Equation (2.9). The π phase shifting length ($L_π$) is calculated by Equation (1.10). Free carrier absorption coefficient change (Δα) is calculated by Equation (1.9). Free carrier absorption loss ($α_π$) on the π phase shifting length is calculated by Equation (2.12).

In order to find a suitable doping concentration for phase shifting, refractive index change and π phase shifting length must be taken into account. Table 2.1 shows the max depletion region width, refractive index change when the MOS capacitor is in the max depletion mode and the π phase shifting length for typical doping concentrations of n-type silicon. As shown in Table 2.1, high doping density results in a large refractive index change and a relatively short phase shifting length. However, the max depletion region width is also small in this case. A low doping

concentration has opposite results. Thus, it is quite important to find a balance among electrical performance, optical performance and size of the device. Considering all the issues including optical loss due to carrier absorption, depletion region width, power consumption and π phase shifting length, 1×10^{17} cm^{-3} is chosen as a suitable doping concentration for n-type MOS capacitor phase shifter working in depletion mode. It has a max depletion region width of 102.6 nm and a π phase shifting length of 18.9 mm. As a result, π phase change can be achieved in a relatively short distance without high carrier absorption loss (7 dB), large dispersion and high driving voltage.

In order to keep the modulator small and compact, some optical enhancement techniques can be used to reduce the π phase shifting length, such as slow light effect in photonic crystal waveguides [62]. In the case of slow light photonic crystal waveguides, if, for example, the slow light enhancement is S=10, then the phase shifting length with doping concentration of 1×10^{17} cm^{-3} is only 1/10 of 18.9 mm, which is 1.89 mm. To reduce the phase shifter length further, slow light PhC waveguides with larger slow down factor should be used. However, this also reduces the bandwidth.

Once the doping concentration is decided, the remaining question is how the MOS capacitor phase shifter performs with a given doping concentration of the silicon substrate. It is a complicated issue. Electrical simulations have been carried out to find out the answer.

2.2 MOS capacitor phase shifter electrical simulation

The electrical performance of the MOS capacitor phase shifter was modelled. The depletion region behaviour, carrier density distributions and capacitance were simulated using a commercial electrical simulation tool, Synopsys TCAD version D-2010.03.

2.2.1 Synopsys TCAD introduction

Synopsys TCAD is an industrial standard electrical simulation package based on a finite element method. It comprises several tools, including device structure building, simulator and virtualization tools.

2.2.2 Physics model

Sentaurus Device is a device modelling tool for electrical performance simulation. It offers a set of physics models for semiconductor devices modelling. The major physics models used in this simulation are electrostatic potential, quasi-Fermi potential with Fermi-Dirac statistics and carrier transport model. In semiconductor devices, mobile charges (electrons and holes) and immobile charges (ionized dopants or traps) determine the electrostatic potential. However, in turn, they are also affected by the electrostatic potential. As the charges are the key factors that influence the performance of the semiconductor devices, the

electrostatic potential and the quasi-Fermi potentials which describe the electron and hole densities are the essential physics models used in the MOS capacitor phase shifter simulation.

For a given charge distribution, electrostatic potential is solution of the Poisson equation, which is [63]:

$$\nabla \cdot (\varepsilon \nabla \phi + \vec{P}) = -e(N_h - N_e + N_d - N_a) - \rho_{trap} \quad \textbf{(2.13)}$$

where ε is the electrical permittivity, $\vec{P}$ is the ferroelectric polarization, e is the electronic charge, N_e and N_h are the electron and hole densities, N_d is the donor concentration, N_a is the acceptor concentration, ρ_{trap} is the charge density contributed by traps and fixed changes.

If Fermi-Dirac statistics is assumed, electron and hole densities can be calculated from electron and hole quasi-Fermi potentials, which are given as

$$N_e = N_C F_{1/2}\left(\frac{E_{F,n} - E_C}{kT}\right) \quad \textbf{(2.14)}$$

$$N_h = N_V F_{1/2}\left(\frac{E_V - E_{F,p}}{kT}\right) \quad \textbf{(2.15)}$$

where N_C and N_V are the effective density-of-states, $F_{1/2}$ is the Fermi integral of order 1/2, $E_{F,n}$=-eϕ_n and $E_{F,p}$=-eϕ_p are the quasi-Fermi energies for electrons and holes, ϕ_n is electron quasi-Fermi potentials, ϕ_p is hole quasi-Fermi potentials, E_C and E_V are conduction and valence band edges.

Carrier transport model describes the motion of free carriers in a semiconductor caused by an external electric field and thermal energy, which is given as

$$\nabla \cdot \vec{J}_n = eR_{net} + e\frac{\partial n}{\partial t} \quad \textbf{(2.16)}$$

$$-\nabla \cdot \vec{J}_p = eR_{net} + e\frac{\partial p}{\partial t} \quad \textbf{(2.17)}$$

where R_{net} is the net recombination rate, $\vec{J}_n$ is the electron current density, and $\vec{J}_p$ is the hole current density.

	W_{total} /um	W_n /um	W_p /um
Simulated	**~1.5**	**~1.4**	**~0.1**
Calculated	**1.58**	**1.43**	**0.14**

Table 2.2 Theoretically calculated and simulated depletion region width of a silicon PN junction. W_{total} is the total depletion region width, W_n is the depletion region width in the n region and W_p is the depletion region width in the p region. The calculated results are obtained from Equation (1.14) - (1.16). The donor concentration is 5×10^{15} cm^{-3} and the acceptor concentration is 5×10^{16} cm^{-3}. The reverse biased voltage is 8 V.

The physics model is verified by a simulation of a simple silicon PN junction. The donor (n-type) concentration is 5×10^{15} cm^{-3} and the acceptor (p-type) concentration is 5×10^{16} cm^{-3}. The p and n regions are uniformly doped and the transition between the two regions is abrupt. A reverse bias (V_a=8V) is applied to the

PN junction. The simulated total depletion region width is ~1.5 um, the depletion region width in the n region is ~1.4 um and that in the p region is ~0.1 um. These results match the theoretical calculations very well (see Table 2.2) and give us confidence to use the model in the silicon MOS capacitor phase shifter simulation.

2.2.3 Simulation structure and settings

Simulated structure is the electrical part of the phase shifter, a MOS capacitor. The aim of the simulation is to model the depletion region and capacitance behaviours with the applied DC voltage. The schematic diagram of the simulated structure is shown in Fig.2.5. The device is a 3D structure with 1 um in the z direction as default. Silicon used in the simulation is 220 nm thick, which is the same with the top layer of silicon-on-insulator (SOI). Buried oxide (BOX) and silicon substrate underneath are ignored in the simulation for convenience and time saving. The silicon substrate is p-type doped with the doping density of 3×10^{17} cm^{-3}. It should be noted that the dopant type does not affect the depletion region width and capacitance, which is determined by the doping concentration and the applied voltage. Therefore, the simulations based on p-type silicon substrate are also useful for the device with n-type silicon. SiO_2 is used as a gate oxide with thickness of 100 nm. The width of SiO_2 is reduced to half of its real size (250 nm instead of 500 nm), also to save simulation time.

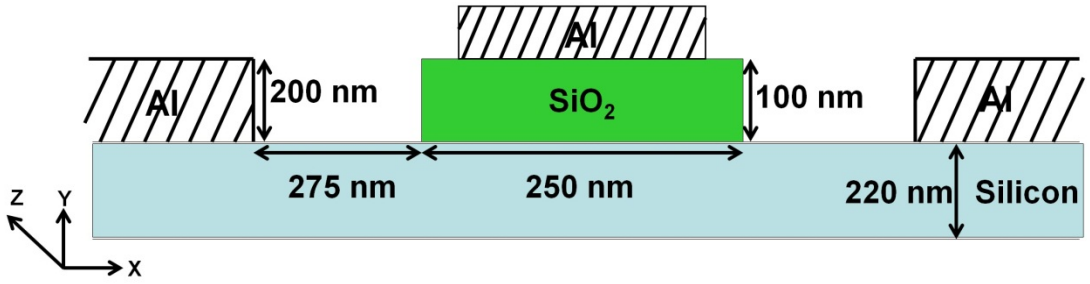


Fig.2.5 Schematic diagram of the simulated phase shifter. SiO_2 is used as a gate oxide with thickness of 100 nm. Aluminium (Al) contacts are on top of SiO_2 and also on the silicon at the two sides. The silicon is p-type doped with a doping concentration of 3×10^{17} cm^{-3}.

The mesh settings are 10 nm in the x direction, 5 nm in the y direction and 50 nm in the z direction. The element size in the z direction is much larger than the x and y direction as the result in the z direction is less important than the other two directions. Detailed settings and scripts written in tool command language (Tcl) are listed in the appendix. 3.9, as a typical value of dielectric constant of SiO_2, was used in the simulation and theoretical analysis. In order to model the depletion region of the p MOS capacitor, positive voltages are applied to the Al central contact, while the two side Al contacts are both grounded.

2.2.4 Simulation results and discussion

Depletion region width and capacitance-voltage (C-V) characterization were modelled with different DC voltages. Fig.2.6 shows the distributions of the electric field absolute values and also the depletion region width at +10 V.

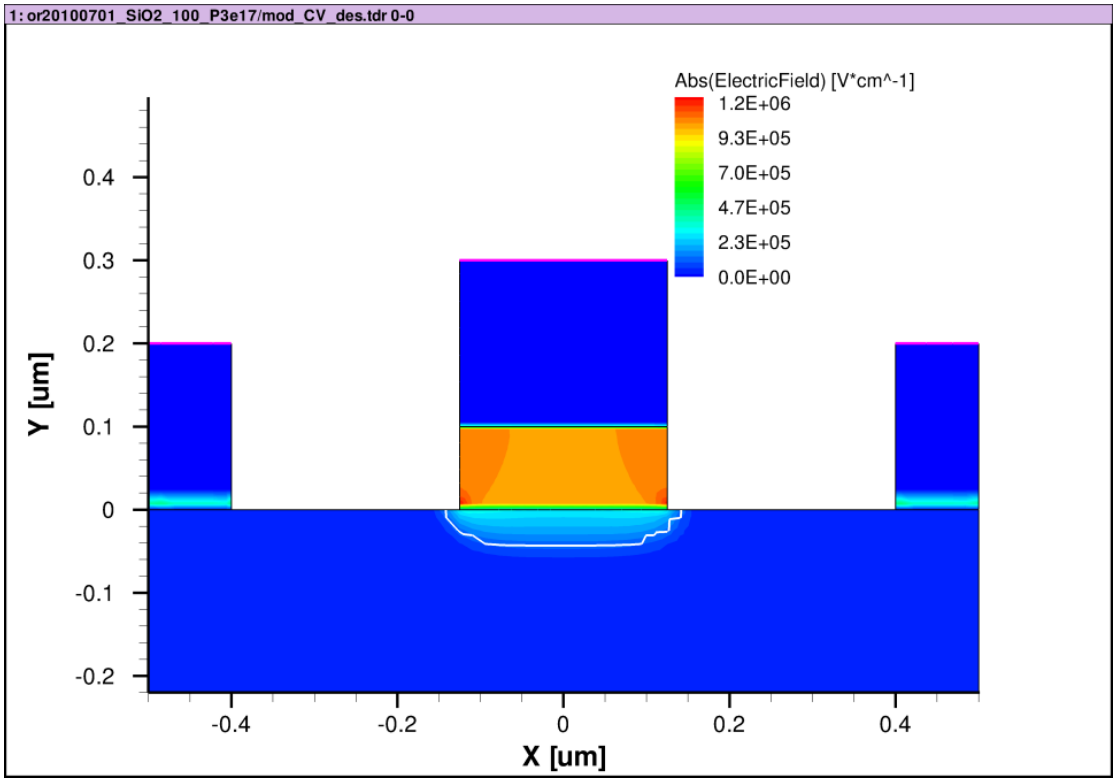


Fig.2.6 Simulation results of electric field distribution in the device. The voltage applied to the gate contact is +10 V. The white line indicates the boundary of the depletion region. The depletion region width is around 45 nm.

From Fig.2.6, the depletion region width of the MOS capacitor with 100 nm SiO_2 at +10 V is about 45 nm. According to Equation (2.6), the maximum depletion region width of doping concentration of 3×10^{17} cm^{-3} is 61 nm. It is quite obvious that +10 V is not enough to achieve the maximum depletion region width. By increasing the applied positive voltage to +25 V, the depletion region width increases to 60 ~ 70 nm (see Fig.2.7). In this case, the simulated maximum depletion region width matches the theoretically calculated result.

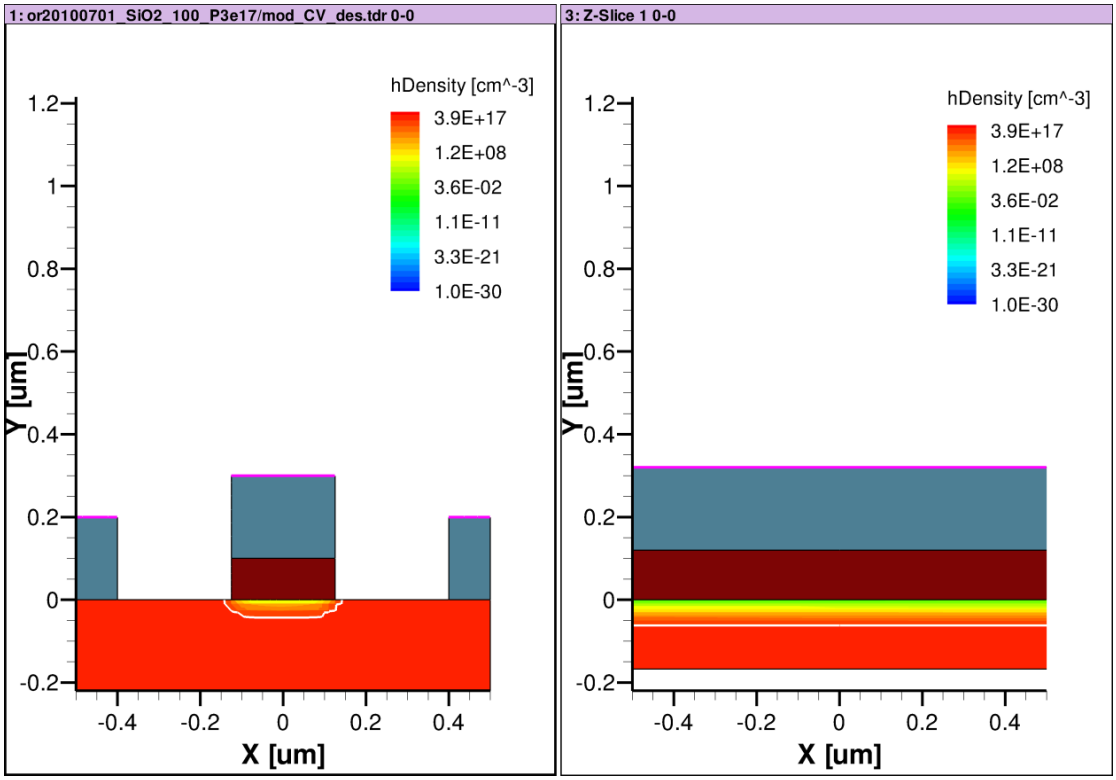


Fig.2.7 Hole density distribution in the MOS capacitor at +25 V. The left figure shows the hole density distribution in the whole device. The left figure shows the hole density distribution around the SiO_2-Si interface. The two figures show that the positive voltage pushes the holes away from the SiO_2-Si interface and then the depletion region occurs.

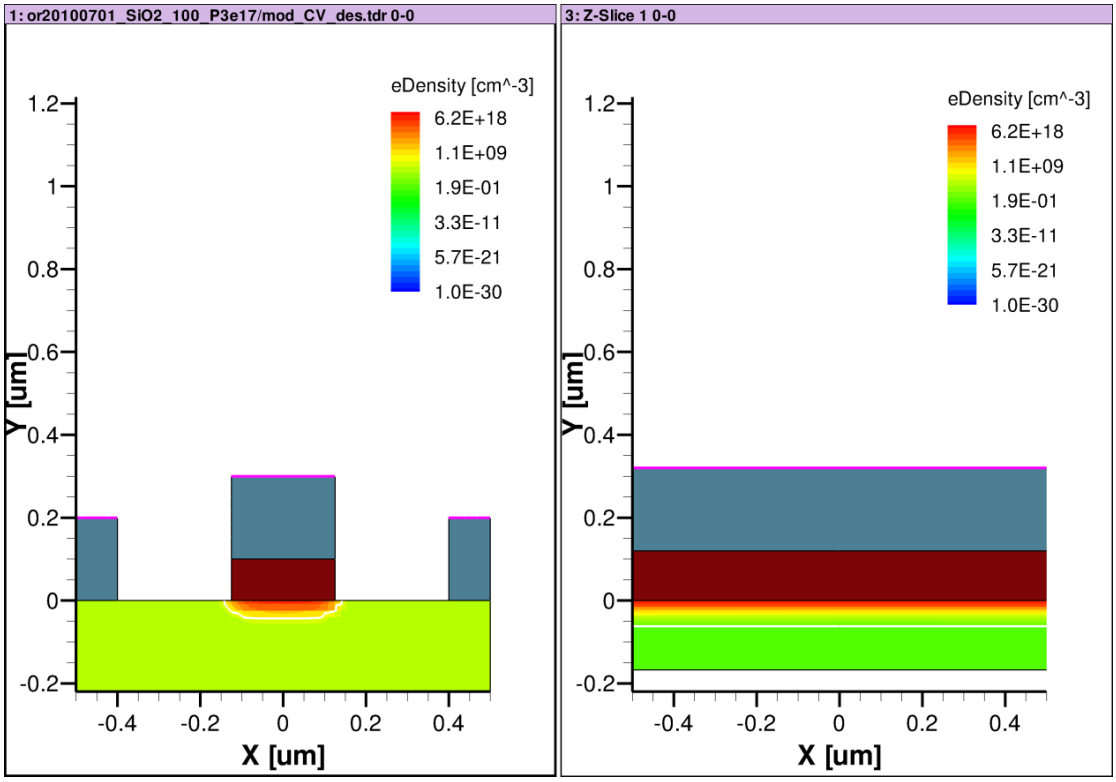


Fig.2.8 Electron density distribution in the MOS capacitor at +25 V. The left figure shows the electron density distribution in the whole device. The left figure shows the electron density distribution around the SiO_2-Si interface where the inversion layer occurs.

As shown in Fig.2.7 and Fig.2.8, the maximum depletion region width is relatively small with the p-type doping concentration of 3×10^{17} cm^{-3}, which is around 60 nm, less than 1/3 of the silicon layer thickness. In this case, the overlap between the optical mode and the depletion region is small, which results in dispersion and distortion. The best situation is that the waveguide region is fully depleted and then, the entire optical mode in the waveguide experiences the same refractive index change. Nonetheless, the reality is that if this happened, the doping concentration would be too small to make a large carrier density change. Hence, the phase shifter

must be long to have a π phase change. The longer length brings more propagation loss. Hence, it is better to use silicon with moderate doping concentration, which has a suitable maximum depletion region width, a relatively short π phase shifting length and a small total free carrier absorption loss.

Fig.2.7 and Fig2.8 also clearly show that the majority carriers (holes) are pushed away from the SiO_2-Si interface by positive gate voltage, while a thin layer of minority carriers (electrons) occurs at the silicon side of the SiO_2-Si interface, which is called an inversion layer. The presence of the inversion layer increases the carrier density in the depletion region and consequently, lowers the carrier density change. As a result, the occurrence of an inversion layer should be avoided in the MOS capacitor phase shifter operation.

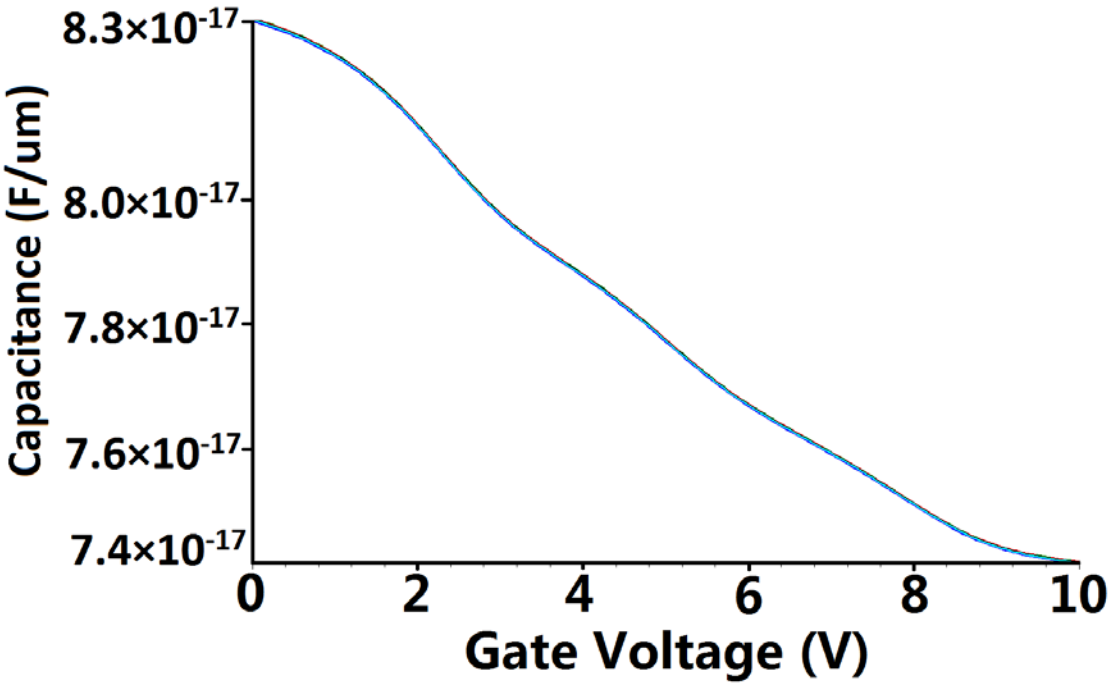


Fig.2.9 Simulation result of C-V characterization of the MOS capacitor phase shifter. The capacitance is of 1 um long device in the z direction.

Fig.2.9 shows C-V characterization of the MOS capacitor phase shifter. The simulated capacitance is of per um long in the z direction. The simulation shows that the capacitance of the device is in the order of 10^{-17} F/um. Theoretical calculated capacitance and simulated capacitance of the device along the z direction are 7.17×10^{-17} F/um and 7.4×10^{-17} F/um, respectively. The calculated capacitance is based on Equation (2.5). The area of the MOS capacitor is 250 nm × 1 um. The simulated capacitance is obtained from C-V curves in Fig.2.9 at the applied voltage of +10 V. The simulated capacitance is slightly larger than the theoretical result. This is because the depletion region does not reach its maximum width. The C-V curve shows that the capacitance decreases with the increasing depletion region width. This result agrees with the theoretical analysis (Equation (2.5)). For a 100 um long phase shifter, the corresponding capacitance is in the order of 10 fF, which is as close to the capacitance (25 fF) of the recently reported modulator with a similar footprint [64].

2.3 Conclusion

A theoretical analysis of the n-type phase shifter based on a MOS capacitor in depletion mode has been discussed. The maximum depletion region width, refractive index change, effective refractive index change, π phase shifting length, absorption coefficient change and absorption loss on the π phase shifting length for typical doping concentration values have been calculated. The effective refractive index change calculation is based on a coarse assumption in which the overlap

between depletion region and optical mode is the ratio between the depletion region width and the silicon layer thickness. However, it shows the orders of magnitude and the its relation with the doping concentration.

In summary, the MOS capacitor phase shifter with SiO_2 as a gate oxide has a relatively small capacitance per unit length (~10^{17} F/um), which is good for high speed modulation. The simulation results and the theoretical analysis agree each other very well on the MOS capacitor depletion region width and capacitance. For high speed modulation, the driving voltage of 10 V and 25 V is too high, because too much Voltage drops across the gate oxide (insulator). However, when the gate oxide is thinner, the metal contact on top gets closer to the waveguide. Consequently, optical losses due to metal absorption increase significantly. Therefore, a transparent conducting layer with both electrical conductivity and optical transparency can be introduced between the metal contact and the gate oxide to improve electrical performance without losing optical isolation.

Based on the theoretical analysis and simulated result, n-type silicon with a doping concentration of 1×10^{17} cm^{-3} is chosen as the phase shifter substrate. It has a maximum depletion region width of 103 nm which is almost half of the silicon layer thickness, a moderate effective refractive index change of 4.11×10^{-5}, a relatively short π phase shifting length (1.9 mm after the slow light enhancement) and relatively small total loss (7 dB) due to free carrier absorption in the silicon waveguide.

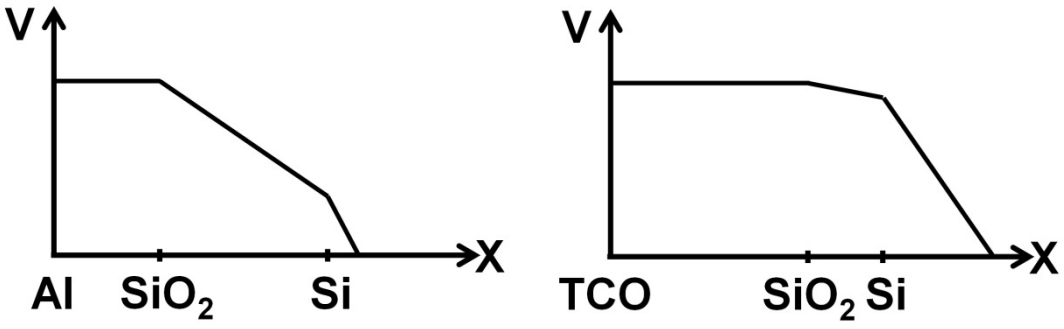
Chapter 3

Transparent Conducting Oxide, ITO Fabrication & Transmittance Characterization

3.1 Transparent conducting oxide

In chapter 2, the simulation result shows the electrical performance of the MOS capacitor phase shifter with SiO_2 as a gate oxide. However, SiO_2 is an insulator. A metal layer must be placed on SiO_2 as an electrical contact and consequently produces strong metal absorption. This can be conquered by using a thicker SiO_2 to improve the optical isolation. Nevertheless, the thicker SiO_2 also increases the electrical isolation in which case larger voltages are needed to deplete the silicon underneath (Fig.3.1(a)). Therefore, instead of a thick SiO_2 layer between the Al contact and silicon waveguides, transparent conducting oxide (TCO) material which has both electrical conductivity and optical transparency should be used as a transparent electrode on top of a thin SiO_2 layer (see Fig.3.2). By using a TCO/SiO_2/Si

structure with a thinner SiO_2 layer, the potential that drops on the isolation layers (TCO and SiO_2) can be reduced (Fig.3.1(b)). Besides, optical losses due to the TCO layer are much smaller than those due to metal absorption from the Al contact.



(a) (b)

Fig.3.1 Potential Distribution in Al/SiO_2/Si and TCO/SiO_2/Si Structures. (a) shows that in Al/SiO_2/Si structure, the applied voltage mainly drops across the SiO_2, as SiO_2 is an insulator. In this situation, large voltage is needed to achieve the desired depletion region width. (b) shows that by using the transparent conducting oxide, the thickness of SiO_2 can be reduced. Therefore, the driving voltage mainly drops on the silicon, in which case smaller voltage can do the same operation.

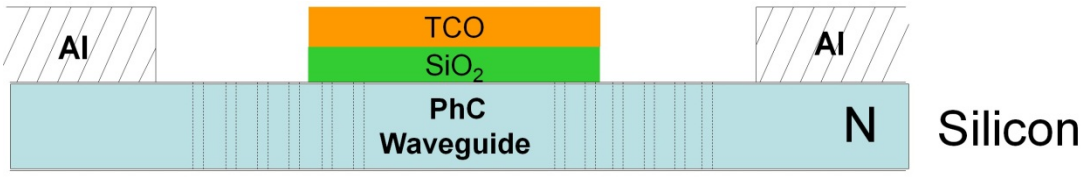


Fig.3.2 Cross-sectional view of the silicon MOS capacitor phase shifter with transparent conducting oxide (TCO). A thin TCO layer is used as a transparent electrode above the gate oxide (SiO_2).

3.2 ITO properties

Indium Tin Oxide (ITO) as a transparent conducting material, was chosen for the silicon electro-optic modulator because ITO has both electrical conductivity and optical transparency in the visible and near infrared (NIR) range [65-68]. It is tin-doped indium oxide (In_2O_3) and has been widely used as transparent conductor in many optoelectronic devices such as solar cells, liquid crystal displays (LCD) and gas sensors etc. [69-73]. ITO has a dielectric constant (ε=9), a mobility of 100 $cm^2/V{\cdot}s$ and a carrier density in the order of 10^{20} cm^{-3} [74,75]. Electrical and optical properties of ITO are strongly related to doping levels, fabrication method and annealing process. Many methods have been reported on the deposition of ITO films, such as sputtering, thermal evaporation, electron beam evaporation, spray pyrolysis, pulsed laser deposition (PLD) and screen printing etc. [76-80]. We have chosen to use the electron beam evaporation as it is readily available in our laboratory.

Indium oxide is optically transparent and electrically insulating when it is pure. By doping with tin as donor, indium oxide becomes ITO and gains electrons to become electrical conductive [81]. Therefore, ITO is an n-type degenerated semiconductor [82,83]. Sheet resistance of ITO varies between a few to thousands of Ω/□ depending on free carrier concentration, mobility and film thickness. Thus, electrical properties of ITO are strongly related to fabrication process.

Regarding to optical properties of ITO, it is highly transparent in visible and near infrared region and it also has high reflection in infrared range (2.5 ~ 15 um)

[84,85]. Transmittance of ITO at NIR wavelengths is determined by free carrier concentration, as free carriers have a strong absorption in the NIR [86,87]. Refractive index of ITO is around 1.7 [88].

In summary, ITO as a transparent conductor is promising for the phase shifter. However, special attention must be paid in the fabrication process in order to achieve good performance.

Phase Shifter Structure	**ITO/SiO_2/Si**	**Al/SiO_2/Si**
SiO_2 Thickness /nm	**50**	**300**
Capacitance /F	**7.75×10^{-12}**	**1.95×10^{-12}**

Table 3.1 Theoretically calculated capacitance of the MOS capacitor phase shifter in two different structures. The calculation is according to Equation 2.5. The phase shifter structure is shown in Fig.3.2 (ITO/SiO_2/Si) and Fig.2.1 (Al/SiO_2/Si). The doping concentration of n-type silicon substrate is 1×10^{17} cm^{-3}. The width of the SiO_2 layer is 10 um to cover the photonic crystal waveguide and the length is 1.89 mm which is the full length of the slow light PhC phase shifter discussed in chapter 2. The thicknesses of SiO_2 for the two structures are 50 nm and 300 nm.

The capacitance of the two MOS capacitor phase shifter structures (Al/SiO_2/Si and ITO/SiO_2/Si) based on the design in Fig.2.1 is calculated from Equation 2.5. The length of the phase shifter is 1.89 mm which has been discussed in chapter 2. The result is shown in Table 3.1. The calculated capacitance of both structures is in the same order (10^{-12} F), but the structure with ITO has a larger capacitance than the other one. This is because the capacitance of a MOS capacitor

increases with the decreasing oxide thickness. This calculation neglects the capacitance contributed by the ITO layer. One reason is because the ITO layer is very thin (<= 100 nm). The second reason is that when ITO is used as a conductor, its influence on the capacitance is relatively small, just like Al.

3.3 ITO fabrication

The ITO film is deposited by electron beam evaporation from ITO powder in the crucible. The ITO powder is from Testbourne Ltd. with In_2O_3 : SnO_2 = 90 : 10 wt%. As ITO's electrical and optical properties are greatly affected by the free carrier concentration and mobility which are determined by the fabrication process, the actual issue is how to control free carrier concentration and mobility during the fabrication.

There are several ways to control free carrier concentration and mobility, including using angled deposition, controlling deposition rate and post-deposition annealing. During the electron beam deposition, the ITO vapour contains some In and Sn metal particles. They work as donors in the deposited ITO film and provide extra free carriers. The ITO film deposited with the incident angle (the ITO vapour to the sample) of 45˚ has lower free carrier concentration than that deposited with the incident angle of 0˚, as the metal indium particles are greatly reduced in this case. Fig.3.3 shows the ITO deposition at 45˚. Low deposition rate could also reduce In and Sn impurities in the ITO film, because in this way, In and Sn particles are exposed to O_2 molecules in the vacuum chamber for longer and are more likely to become oxides [89]. As a result, optical loss due to metal absorption is lowered and

transmittance of the ITO film is enhanced. It was reported that transmittance of the ITO film deposited at incident angles of 0˚ and 45˚ are 89% and 93% at the wavelength of 800 nm after annealing at 450˚C in air [90]. During the ITO deposition, the rate is controlled at 0.01 nm/s and never gets higher than 0.03 nm/s. The post-deposition annealing in air oxidizes the remaining metal particles in the ITO film. Moreover, it transforms ITO microcrystals into ITO large crystals, which increases the free carrier mobility in the ITO film. The ITO film looks dark and opaque on the glass after deposition. However, it quickly turns clear and transparent in the first few minutes during the annealing. The ITO film in a well-oxidized state has high optical transmittance as metal absorption has been diminished.

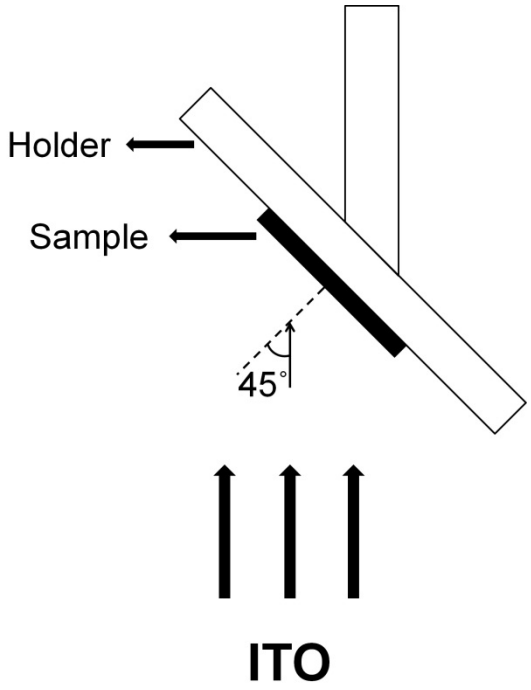


Fig.3.3 45˚ ITO evaporation. Angled deposition reduces the metal particles in the deposited ITO film and decreases optical loss due to metal absorption.

3.4 ITO optical loss test

3.4.1 ITO annealing - transmittance characterization & sheet resistance measurement

In order to test the ITO post-deposition annealing effect on its optical transparency, 140 nm ITO was deposited at 45˚ onto a clear glass slides, annealed at different temperatures and times in air and then the transmittance measured by the spectrometer. The clear glass slides were cleaned by acetone, isopropyl and deionized (DI) water before loading into the evaporator. The ITO deposition was done by the electron beam evaporator at 45˚ with the rate at 0.01 - 0.03 nm/s. The glass slides with ITO on one side were annealed in the hotplate exposed in air with different temperatures and times. Then ITO thicknesses were measured with a Dektak 150 Stylus Profiler. Finally, the transmittance of glass slides with ITO was measured by the Perkin Elmer Lambda 950 UV/VIS Spectrometer, using a piece of cleaned clear glass slide or air as references. The transmittance equals I_f/I_r where I_f is the optical power through the ITO film on a glass slide and I_r is the optical power through the reference object (air or a clear glass slide). Fig.3.4 shows the transmittance measurement system.

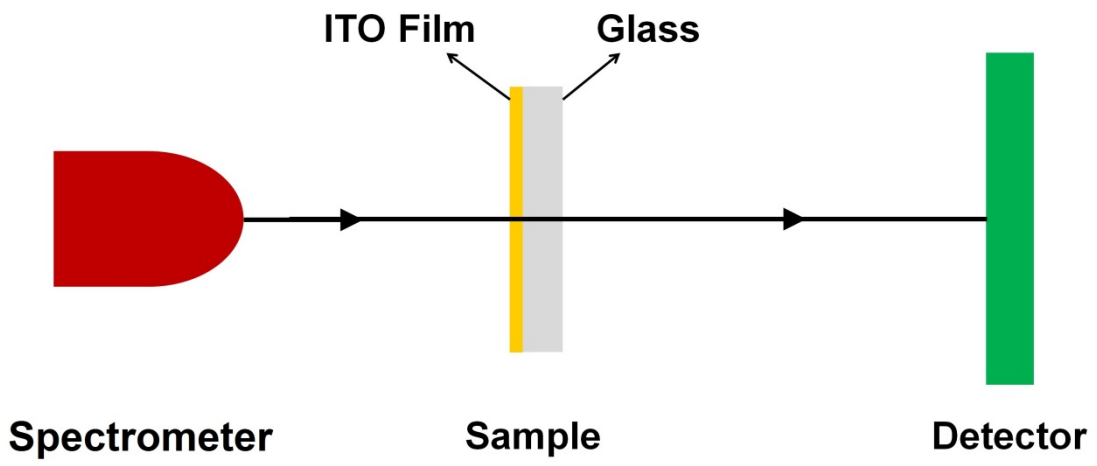


Fig.3.4 Transmittance measurement of the ITO film on a glass slide. The whole system contains a spectrometer and a photodetector. The transmittance equals I_f/I_r where I_f is the optical power through the ITO film on a glass slide and I_r is the optical power through the reference object (air or a clear glass slide).

The sheet resistance was also measured by the four probe sheet resistance measurement system (Jandel RM3-AR). Table 3.2 shows the results of annealing temperature, annealing time, transmittance and sheet resistance. The annealing was in air at the temperature from 350˚C to 500˚C. These temperatures are most likely to have both high transmittance and low sheet resistance according to the literatures [89,90].

From Table 3.2, it is easy to find that for the ITO transparent conductor, the ideal combination is the highest transmittance and the lowest sheet resistance. During the experiment, annealing with higher temperature (over 500 ˚C) and longer time did not improve the electrical and optical performance of ITO film. According to the test result, the best combination appears at “350C30m_400C30m” when the sample is annealed at 350˚C for 30 minutes and 400˚C for another 30 minutes, in

which case the transmittance at wavelength of 1550 nm is around 87.9% referring to air and the sheet resistance is 730 Ω/□. These measurements were repeated several times. We got roughly the same results with the same conditions. It should be noted that ITO transmittance also depends on wavelength (see Fig.3.5).

Annealing Condition	Transmittance %	Sheet Resistance (Ω/□)
350˚C 30min	87.5	843.9
350˚C 30min, 400˚C 30min	87.9	729.9
350˚C 30min, 400˚C 60min	86.9	2113
350˚C 30min, 400˚C 60min, 450˚C 30min	87.7	1065.6
350˚C 30min, 400˚C 60min, 450˚C 60min	87.6	1059.1
350˚C 30min, 400˚C 60min, 450˚C 90min	87.8	638.8
350˚C 30min, 400˚C 60min, 450˚C 120min	87.4	1598.8
350˚C 30min, 400˚C 60min, 450˚C 150min	87.5	1905.2
350˚C 30min, 400˚C 60min, 450˚C 150min, 500˚C 30min	87.4	1532.8
350˚C 30min, 400˚C 60min, 450˚C 150min, 500˚C 60min	87.2	1773.8
350˚C 30min, 400˚C 60min, 450˚C 150min, 500˚C 120min	87.6	790.4
350˚C 30min, 400˚C 60min, 450˚C 150min, 500˚C 180min	86.8	1544.6

Table 3.2 Annealing-transmittance-sheet resistance measurement results of the first test of the ITO film on a glass slide. The transmittance was measured at

wavelength of 1550 nm. The sample was annealed and measured continuously. The ITO film is deposited at 45˚. The film thickness is 140 nm. The transmittance is measured referring to air.

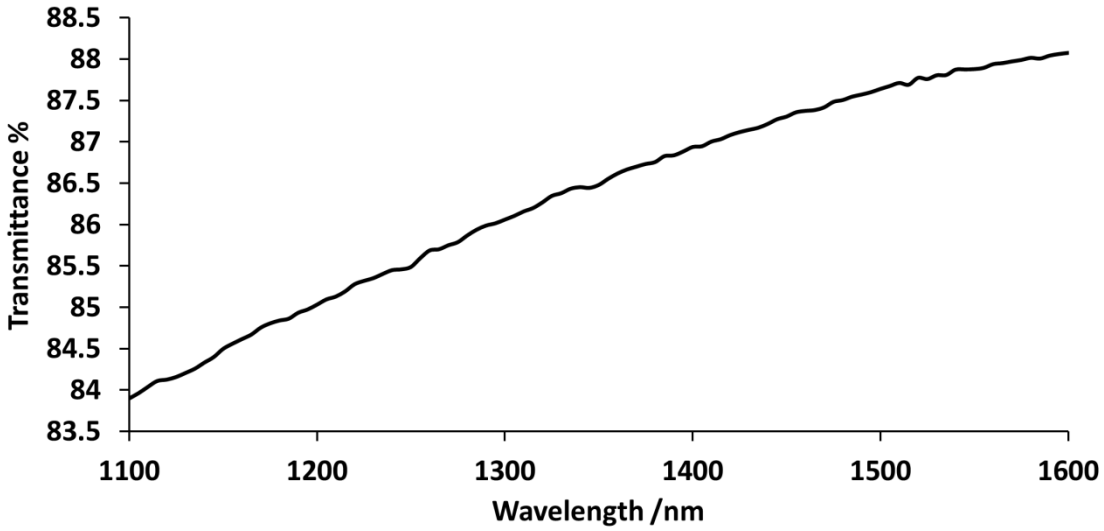


Fig.3.5 ITO transmittance dependence on wavelength. The ITO film with a thickness of 140 nm was deposited at 45˚, annealed at 350˚C for 30 minutes and 400˚C for another 30 minutes. The transmittance at 1550 nm is around 87% referring to air.

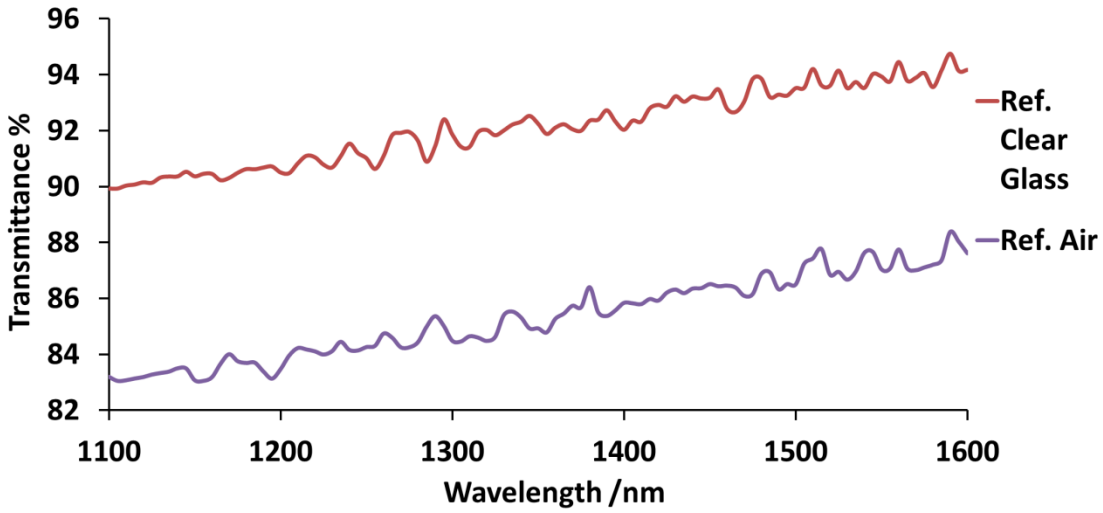


Fig.3.6 The second transmittance measurement test of 140 nm ITO film on glass sample. The ITO was deposited at 45˚ and annealed at 400˚C for 30 minutes in air. The transmittance is around 94% at 1550 nm referring to a clear glass slide. Referring to air, the transmittance is around 87%. Transmittance difference between reference to a clear glass slide and air is because of the reflection and absorption of the clear glass slide.

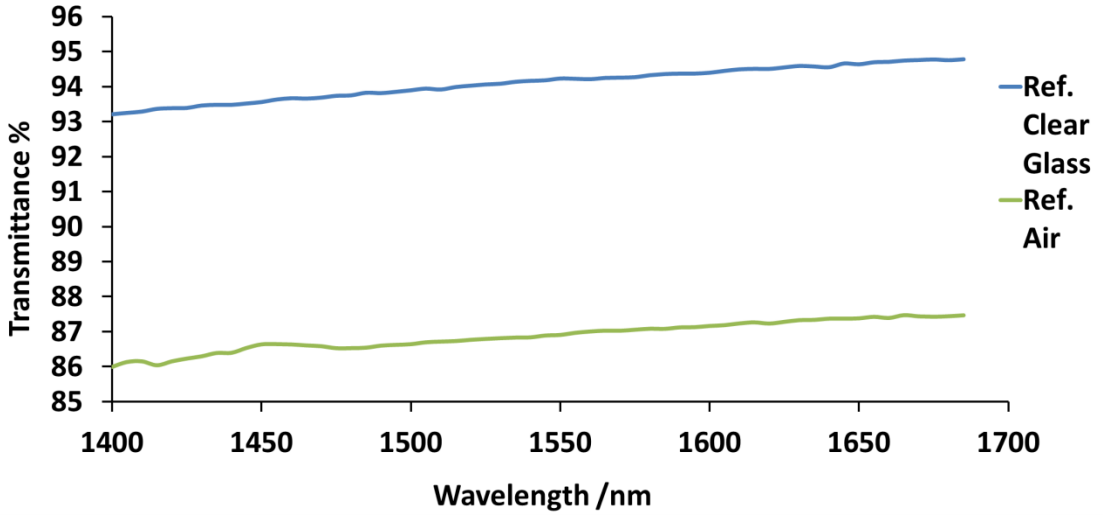


Fig.3.7 The third transmittance measurement test of 140 nm ITO film on glass sample. The ITO was deposited at 45˚ and annealed at 400˚C for 30 minutes in air.

The transmittance is about 94% referring to a clear glass slide. Referring to air, the transmittance is around 87%.

Two more transmittance tests with the same fabrication process were performed in order to make sure that the transmittance at 1550 nm is stable (see Fig.3.6 and Fig.3.7). Transmittance difference between reference to a clear glass slide and air is because of the reflection and absorption of the clear glass slide. Fig.3.6 and Fig.3.7 are from two different samples which were fabricated separately. The results show that the transmittance at 1550 nm is about 94% referring to a clear glass slide and 87% referring to air, which are very close to results of the first test (Fig.3.5). Therefore, the ITO fabrication process is stable and can be trusted.

In the transmittance measurement referring to air, the below equation can be established

$$A_G + T_{Air} + R + A_F = 1 \quad \textbf{(3.1)}$$

where A_G is the absorbed portion by glass slide, T_{Air} is the transmittance of ITO on glass referring to air, R is the total reflectivity and A_F is the absorbed portion by ITO film. In this case, the transmittance is given as

$$T_{Air} = \frac{I_F}{I_{Air}} \quad \textbf{(3.2)}$$

where I_F is the optical intensity through ITO film on a glass slide and I_{Air} is the optical intensity through air. The total reflectivity of Air/ITO/Glass thin film system is given as

$$R = \frac{n_1^2(n_0 - n_s)^2 \cos^2 k_0 h + (n_0 n_s - n_1^2)^2 \sin^2 k_0 h}{n_1^2(n_0 + n_s)^2 \cos^2 k_0 h + (n_0 n_s + n_1^2)^2 \sin^2 k_0 h} \quad \textbf{(3.3)}$$

where n_0=1, n_1=1.7 and n_s=1.5 are the refractive indices of air, ITO and glass, respectively; $k_0=2\pi/\lambda$ is the wavenumber and h=140 nm is the thickness of ITO film.

In the transmittance measurement referring to a clear glass slide, the below equation can be established

$$I_G + I_{RG} + I_{AG} = I_{Air} \quad \textbf{(3.4)}$$

where I_G is the optical intensity through a clear glass slide, I_{RG} is the optical intensity reflected and I_{AG} is the optical intensity absorbed by glass. The transmittance referring to a clear glass slide is given as

$$T_G = \frac{I_F}{I_G} \quad \textbf{(3.5)}$$

where I_G is the optical intensity through a clear glass slide. Combining with Equation (3.2) and (3.5), Equation (3.4) can be written as

$$\frac{I_G}{I_{Air}} + \frac{I_{RG}}{I_{Air}} + \frac{I_{AG}}{I_{Air}} = \frac{T_{Air}}{T_G} + R_G + A_G = 1 \quad \textbf{(3.6)}$$

where $R_G=I_{RG}/I_{Air}$ is the reflectivity of the reference clear glass slide and A_G is the absorbed portion by the glass slide. The reflectivity R_G of Air/Glass system is given as

$$R_G = \left(\frac{n_s - n_0}{n_s + n_0}\right)^2 \quad \textbf{(3.7)}$$

At wavelength of 1550 nm, T_{Air} and T_G are measured as 86.9% and 95.5%. From Equation (3.2), R can be calculated as 5.8% at wavelength of 1550 nm. From Equation (3.7), R_G can be calculated 4%. Therefore, from Equation (3.6), A_G can be calculated 5%. Then, from Equation (3.1), the absorbed portion by ITO film A_F can be obtained 2.3%. The absorption coefficient of ITO film is given as

$$\alpha_{ITO} = \frac{1}{t}\ln(\frac{1}{T_{ITO}}) \quad \textbf{(3.8)}$$

where t=140 nm is the thickness of ITO film and T_{ITO} is the transmittance of ITO film referring to air. Despite the reflection and absorption due to glass slide under ITO film, the transmittance of ITO film T_{ITO} can be written as

$$T_{ITO} = 1 - A_{ITO} \quad \textbf{(3.9)}$$

Combining Equation (3.8) and (3.9), the absorption coefficient of ITO film is calculated about 1700 dB/cm at wavelength of 1550 nm.

3.4.2 ITO absorption loss on blank waveguide test

The ITO on a glass slide transmittance test only shows the optical loss due to light travelling through the 140 nm thick ITO. However, in the electro-optic modulator, the ITO is on the silicon waveguide where the light travelling direction is parallel to the ITO layer. Therefore, a transmission test of ITO deposited on silicon waveguides is necessary to investigate the additional propagation loss incurred.

The silicon substrate is n-type doped with the doping concentration of 1×10^{17} cm^{-3}. The silicon multimode blank waveguides were written by electron beam lithography and etched in reactive ion etching. Then a layer of silicon flowable oxide (FOx) was spun at 7000 rpm on the sample and baked at 400˚C for 4 hours to form a 70 ~ 80 nm thick silicon dioxide (SiO_2) on the blank waveguides. The FOx layer is used as a spacer between the silicon waveguide and the ITO film to minimise optical losses due to the free carrier absorption in the ITO film. After that, 200 um long and 140 nm thick ITO was deposited at 45˚ using the electron beam evaporator. The ITO deposition process was the same as described above. The optical transmission measurement system is shown in Fig.5.12. The light source used is an ASE source (Amonics C+L Band ASE Source) and the optical spectrum analyser (OSA) used is an Advantest Q8384. Fig.3.8 shows the transmission difference between blank waveguides with no ITO and those with ITO on top. The optical loss due to ITO absorption is around 7 dB (at 1550 nm) depending on the wavelength.

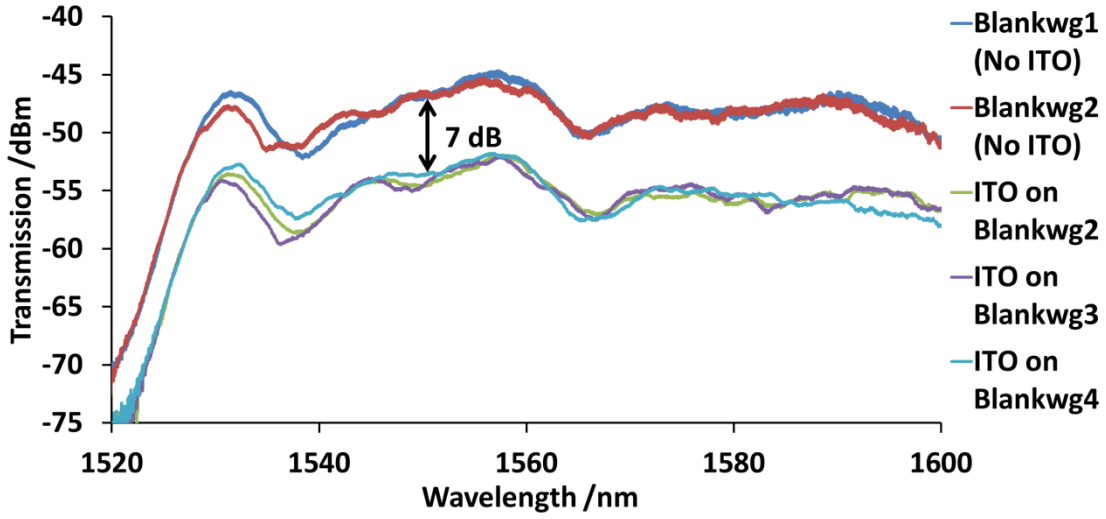


Fig.3.8 ITO on blank waveguide transmission spectra measurement. The optical transmission measurement system is shown in Fig.5.12. The ITO was annealed at

350˚C for 30 minutes and 400˚C for 30 minutes in air. The Blankwg1 (blue) and the Blankwg2 (red) curves are the transmission spectra of two blank waveguides with no ITO. The ITO on Blankwg2 (green), the ITO on Blankwg3 (purple) and the ITO on Blankwg4 (light blue) curves are the transmission spectra of three blank waveguides with 200 um long 140 nm thick ITO on top. The excess loss due to ITO absorption is 7 - 9 dB depending on the wavelength.

In comparison, aluminium absorption loss on blank waveguide has also been tested. 200 nm thick aluminium was deposited directly on silicon blank waveguides. The aluminium covers 180 um long waveguides just as the ITO on blank waveguide test. However, no light can be detected from the aluminium clad blank waveguides during the test. The result shows that the light coupled into the blank waveguide has all been absorbed by aluminium.

3.5 Discussion & conclusion

ITO has good electrical and optical properties and is suitable to use in our phase shifter as the transparent conductor. However, in order to have ideal ITO films, attention must be paid to the ITO fabrication processing. Considering the equipment available, the deposition of ITO at 45˚ with low deposition rate was a suitable method. The post-deposition annealing of ITO at 400˚C for 30 minutes in air has been found to have lowest sheet resistance (~ 700 Ω/□) and highest transmittance (87% referring to air at wavelength of 1550 nm). The absorption coefficient of ITO film with a thickness of 140 nm is about 1700 dB/cm. Resistivity is given as $\rho=R_s t$, where R_s is the sheet resistance and t is the film thickness. Hence, the resistivity of

the deposited ITO film here can be calculated to be ~9.8×10^{-3} Ωcm, which is close to a literature result [90] where the resistivity of ITO film deposited at 45˚ and annealed at 400˚C in air was 5.8×10^{-3} Ωcm. However, compared with those ITO films deposited at normal incidence, whose resistivity is ~10^{-4} Ωcm [91,92], the resistivity of ITO film deposited at 45˚ is relatively large. This is because there is no In and Sn metal particles in the ITO film deposited at 45˚, which lowers the conductivity of the film. The high resistance limits the modulation speed and the performance at high frequencies.

The test result of the transmission measurement of ITO on silicon blank waveguides shows that the 180 um long ITO film results in 7 ~ 8 dB optical absorption loss, due to the free carriers in the ITO film. Assuming that the optical mode in the ITO layer is 1/4 of the total mode, the ITO absorption coefficient can be calculated as (8 dB/180 um)/(1/4)≈1800 dB/cm. This matches the result calculated from the ITO film transmittance.

Although high losses limit the optical performance of the modulator, it does not prevent ITO being used in the phase shifter as a transparent conductor. Furthermore, several advanced fabrication technologies can be used to improve the electrical and optical properties of ITO film, which will be discussed in chapter 6.

In conclusion, ITO has a much lower optical loss than aluminium based on our measurement results. By using ITO instead of Al contact on silicon waveguides, the optical losses can be lowered. Hence, the ITO film as a transparent conducting layer can be used in our phase shifter and modulator design.

Chapter 4

Aluminium – Silicon Contact Characterization

4.1 Aluminium contact fabrication

4.1.1 Aluminium – silicon contact

RC time constant is the key factor for the working speed of an electro-optic modulator. Therefore, it is very important to fabricate low resistance contacts to silicon. As Aluminium (Al) is a good material to form Ohmic contacts with low contact resistance to both n-type and p-type doped silicon, it has been widely used in silicon devices as electrical contacts [93]. In order to measure the Al contact resistance to silicon, a series of contact pads were fabricated and the transmission line method (TLM) was used to determine the contact resistance.

TLM is a technique used to determine the contact resistance between a metal and a semiconductor [94,95]. Fig.4.1 shows the layout used for the TLM measurement. First of all, a series of contact pads are fabricated on the

semiconductor material. Then the probes are applied to the contact pads next to each other. By applying a voltage through the probes, the I-V curves between the two contact pads can be plotted. From this curve, the resistance between the two contacts can be obtained. Once the resistance of each pair of contacts are acquired, the resistance at each separation can be plotted. These are only individual points. Then, the linear trend line can be plotted for these points. The slope of the trend line is the resistivity of the substrate material. The y-intercept is the double contact resistance as the measurement is carried out between two contact pads every time.

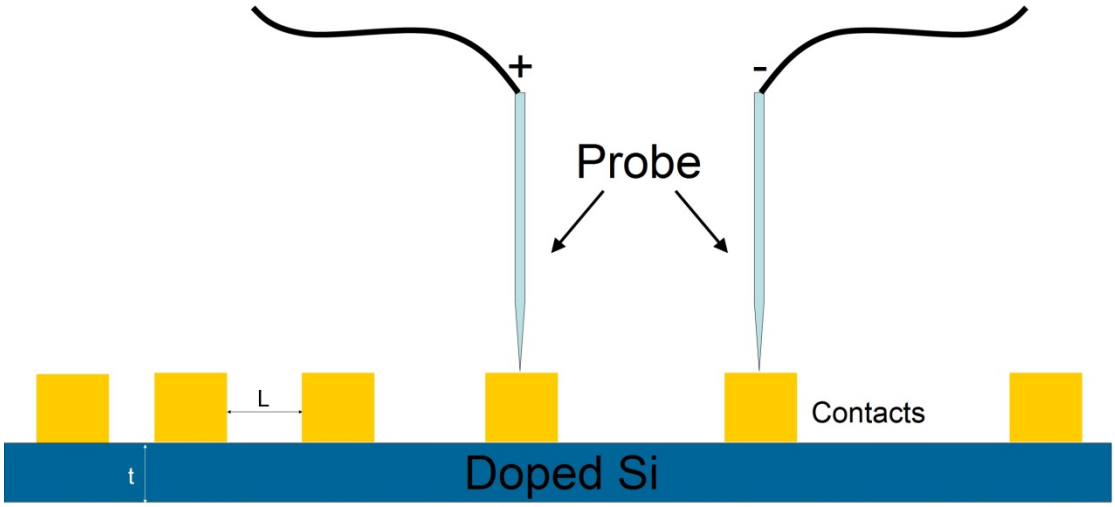


Fig.4.1 TLM measurement. The yellow blocks are the Al contact pads. L is the spacing between each two contacts. t is the thickness of the silicon layer. By using the probes, the resistance between each of two neighbouring contact pads is determined.

4.1.2 Fabrication process

The silicon substrate is SOI with 220 nm thick n-type doped silicon layer. The doping concentration is 1×10^{17} cm^{-3}. To make a good Ohmic contact on the silicon, cleaning the substrate surface is very important, especially removing surface oxide which is the last step before deposition. Firstly, the silicon wafer is cleaned in hot trichloroethylene, acetone and isopropyl alcohol (IPA) using a sonic bath. Then the sample is cleaned in hot aqua regia solution (HCl : HNO_3 = 3 : 1) for 10 minutes to remove metal contaminations. After that, 10 minutes of piranha etch (H_2SO_4 : H_2O_2 = 3 : 1) are performed to remove polymer contaminations. After cleaning in the piranha solution, the windows of the contact pads are opened using photolithography. S1818 G2 is used as photoresist. The sample is exposed under UV light and developed in MF319. Before Al deposition, the sample is cleaned in diluted HF solution (HF : Di water = 1 : 10) for 30 seconds to remove the thin native silicon oxide on the silicon substrate. This step should be very short, as the HF otherwise damages the photoresist and ruins the contact pad windows. Then the sample is loaded into the thermal evaporator for Al deposition. 200 nm Al was deposited. After the deposition, lift-off is then performed in acetone. The final step is the thermal annealing. The annealing is carried out at 450˚C for 5 minutes in N_2 flow. This process is used to reduce the contact resistance, as during the annealing, Al diffuses into silicon and forms an alloy [96,97] (see Fig.4.2).

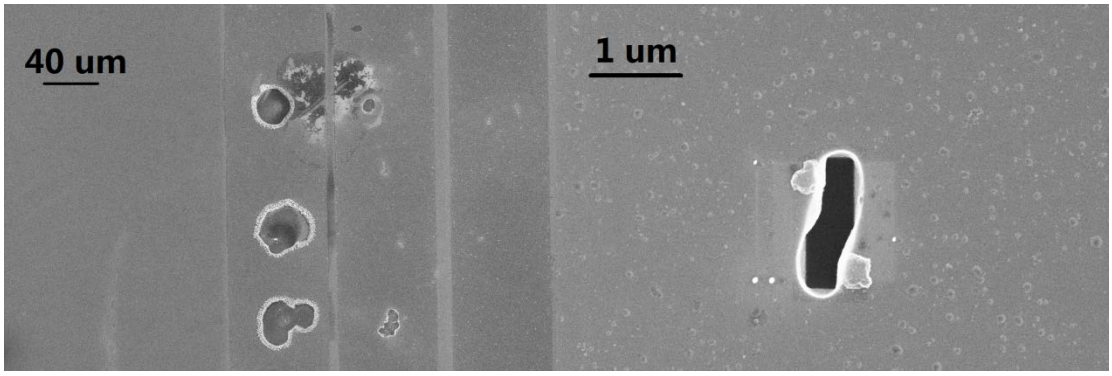


Fig.4.2 SEM images showing the holes caused by Al spiking silicon. The black and dark areas in the images are the holes in silicon. The Al is removed from the silicon substrate in aqua regia after the annealing. The holes in the picture are due to Al spiking in which case Al diffuses into silicon and forms these pits.

4.2 TLM measurement & result

The resistance is measured between two successive contact pads. The contact pads are 500 um long and 200 um wide. The spacing between each two pads is 100 um, 300 um, 500 um, 700 um, 900 um, 1100 um, 1300 um, 1500 um, 1700 um and 1900 um which refer to R_{12}, R_{23}, R_{34}, R_{45}, R_{56}, R_{67}, R_{78}, R_{89}, $R_{9,10}$ and $R_{10,11}$ of the measured resistance (Fig.4.4). The fabricated Al contact pads on silicon substrate for TLM measurement are shown in Fig.4.3. The DC power supply and the multimeter are controlled by a computer program. During the measurement, the current is increased and the voltage measured for each current automatically.

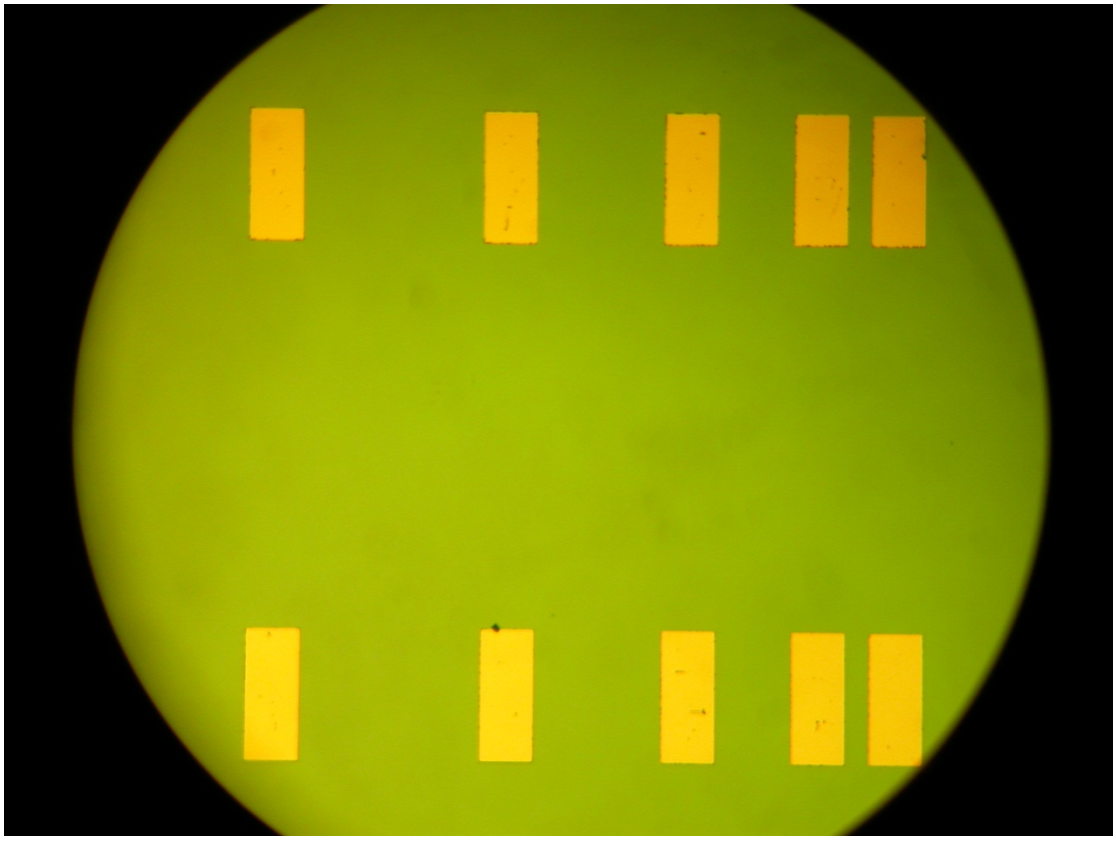
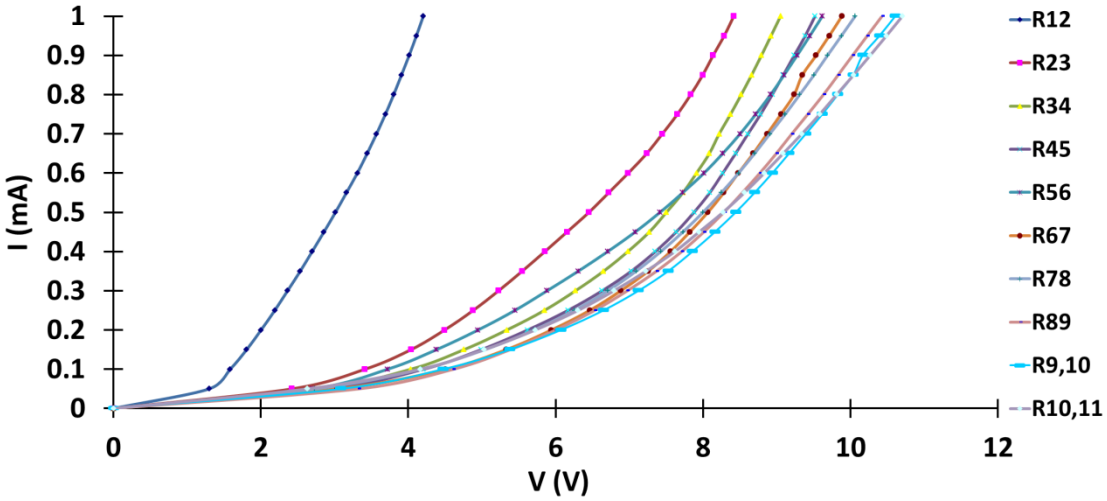
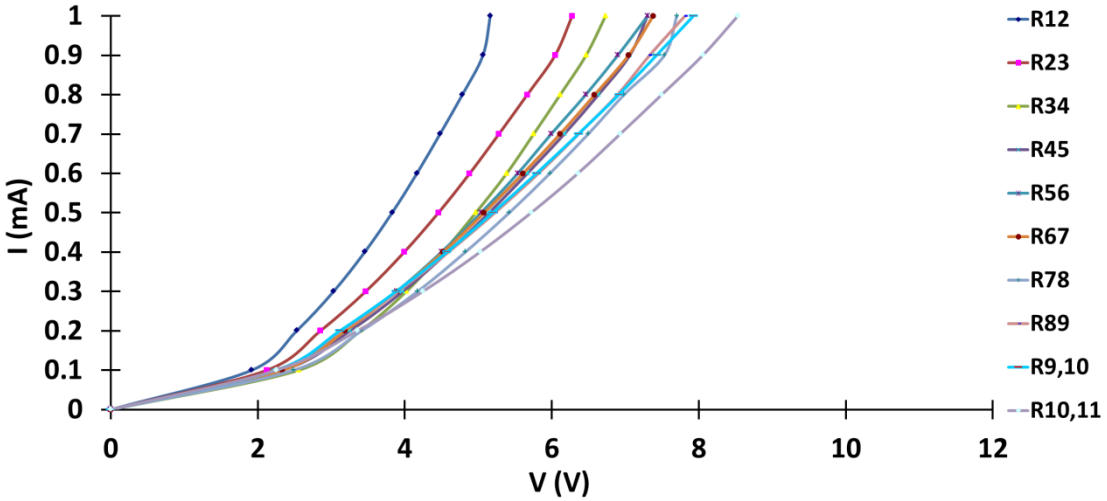


Fig.4.3 Al contact pads on SOI substrate for TLM measurement. The yellow squares are the Al contact pads. The spacing between each two pads is 100 um, 300 um, 500 um, 700 um, 900 um, 1100 um, 1300 um, 1500 um, 1700 um and 1900 um.

Three types of samples were fabricated and measured. The samples were measured before and after annealing to see the corresponding change in contact resistance. Al contact pads were also fabricated on the bulk silicon wafer which is n-type silicon with a thickness of 525 um and a doping concentration of 3×10^{14} ~ 5×10^{15} cm^{-3}. In order to find the influence of the HF cleaning process on the contact resistance, another sample was fabricated and measured without HF cleaning before the Al deposition.



(a) Before annealing



(b) After annealing

Fig.4.4 I-V characterization of n-type 1×10^{17} cm^{-3} SOI sample before (a) and after (b) annealing. No HF cleaning.

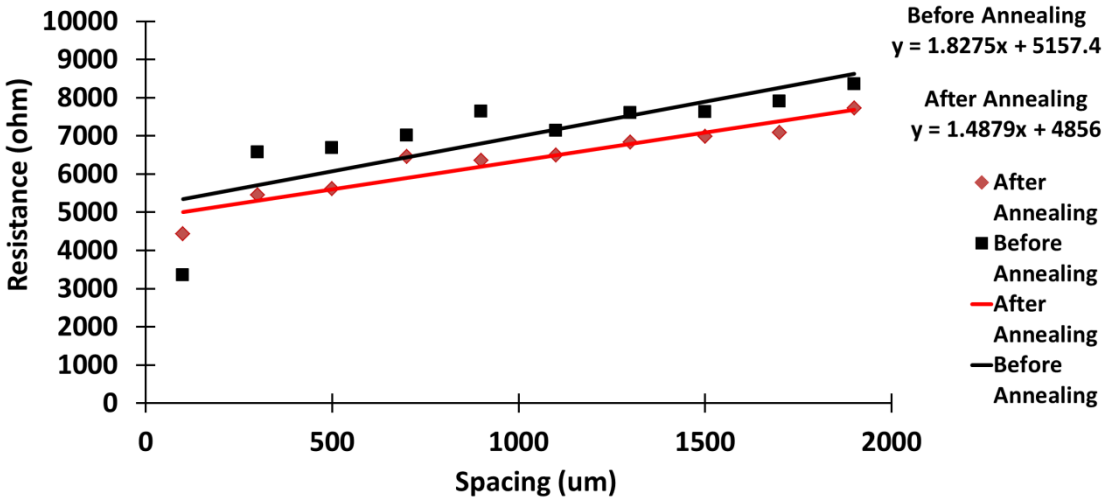


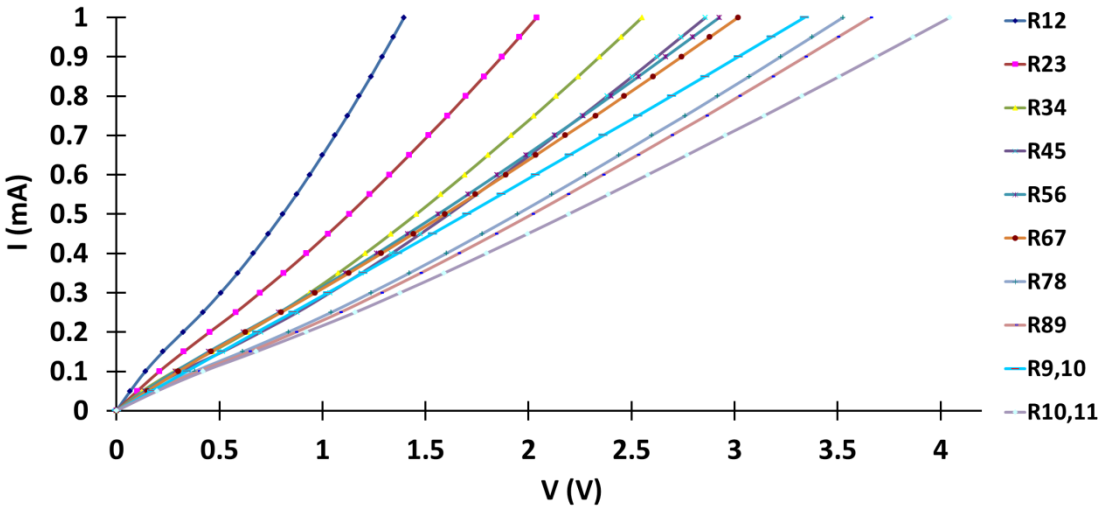
Fig.4.5 Resistance – spacing characterization of n-type 1×10^{17} cm^{-3} sample before and after annealing. No HF cleaning. The curves are linear trend lines of the resistance – spacing points. The equations describe the trend lines. The resistance reduces after the contact annealing.

Contact Resistance /Ω	Before Annealing	After Annealing
No HF Clean	2578.7	2428
HF Clean	860.55	334.93

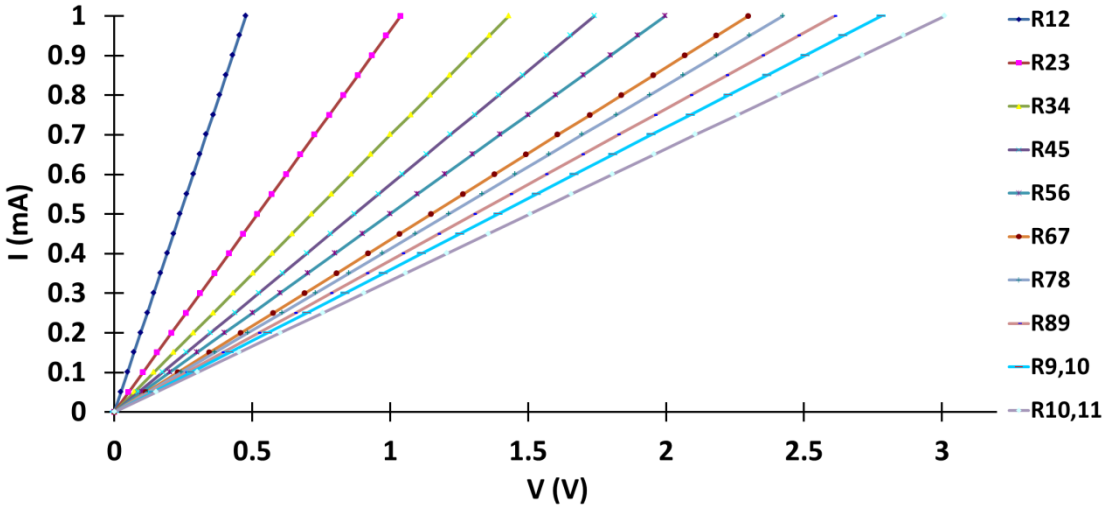
Table 4.1 Contact resistance with and without HF Clean, before and after annealing. The substrate is n-type silicon with a doping concentration of 1×10^{17} cm^{-3}. HF clean and contact annealing help to reduce the contact resistance.

Fig.4.5 and Fig.4.7 show the resistance – spacing relations. The curves are the linear trend lines for each set of points. The equations on the right are for the trend lines. The slope of the linear trend line is the resistivity. The y-intercept represents twice of the contact resistance, as the measurements are carried out between two

contact pads. The obtained contact resistance is shown in Table 4.1. The contact resistance with HF cleaning is much smaller than that without HF cleaning. Before annealing, the HF cleaned contact resistance is 1/3 of that without HF cleaning. However, the HF cleaned contact resistance drops to only 14% of that with no HF cleaning after the annealing. Therefore, the thermal annealing further reduces the contact resistance. Fig.4.4 and Fig.4.6 show the I-V curves of 1×10^{17} cm^{-3} samples with and without HF cleaning, before and after the annealing. The I-V curves shown in Fig.4.4 are measured without HF cleaning, in which case the Al contacts does not work well. Fig.4.6 (a) does not have perfect linear I-V relations. However, after the annealing, Fig.4.6 (b) shows linear I-V relations between each two contacts, which means the annealing process helps the Al contacts to become Ohmic. Comparing Fig.4.4 and Fig.4.6, it is quite clear that the HF cleaning which removes the silicon oxide is also essential to form an Ohmic contact. The Al contacts on low doped silicon (10^{14} – 10^{15} cm^{-3}) do not show linear I-V relations and the contact resistance is a few thousand Ohms, even though the contacts have been cleaned in HF before Al deposition and annealed after Al deposition. This is because Al tends to form Schottky contacts on low doped silicon [98]. Therefore, using a highly doped silicon substrate (>10^{15} cm^{-3}) is quite important for getting Ohmic contacts with low contact resistance [99].



(a) Before annealing



(b) After annealing

Fig.4.6 I-V characterization of n-type 1×10^{17} cm^{-3} sample before (a) and after (b) annealing. With HF cleaning. After contact annealing, the I-V curves become linear and the resistance goes down.

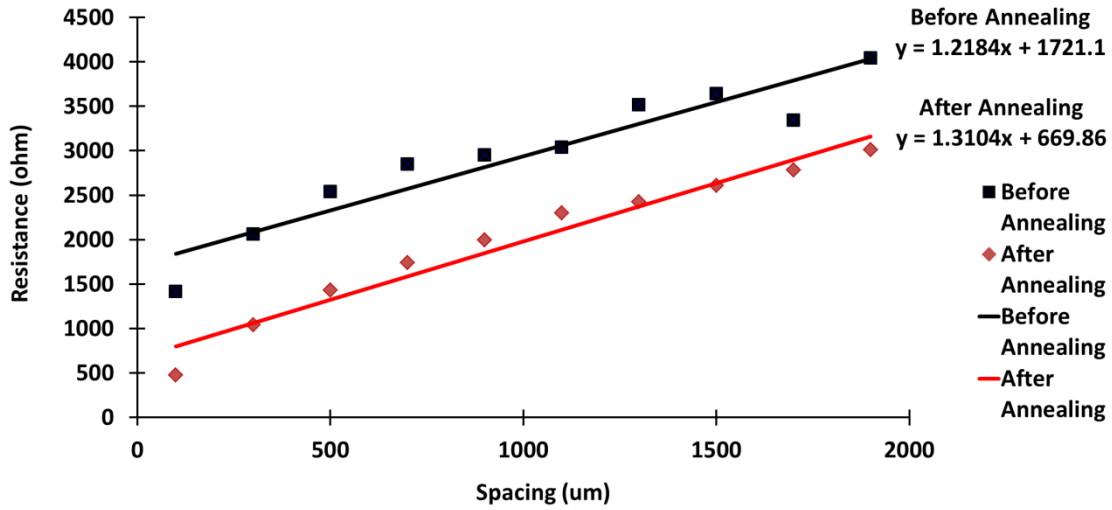


Fig.4.7 Resistance – spacing characterization of n-type 1×10^{17} cm^{-3} sample before and after annealing. With HF cleaning. The curves are linear trend lines of the resistance – spacing points. The equations describe for the trend lines. The resistance reduces after the contact annealing.

4.3 Conclusion

In conclusion, Al can be used in the silicon electro-optic devices as an Ohmic contact to silicon. The contact resistance is around 335 Ω on the n-type silicon substrate with a doping concentration of 1×10^{17} cm^{-3}. When the silicon substrate has a low doping concentration (< 10^{15} cm^{-3}), the Al contact does not work as an Ohmic contact and has high contact resistance. A sufficient substrate doping level, the cleaning process, especially the cleaning in HF, and post thermal annealing are essential to forming good Ohmic contacts with low contact resistance. As the RC time constant is one of the key factors for high speed electro-optic modulator, the contact resistance is preferred to be as small as possible. Several ways can be used to reduce the Al contact resistance to silicon, including a highly doped silicon

substrate in the contact region, and rapid thermal annealing (RTA), which will be discussed in the last chapter.

Chapter 5

Silicon Electro-optic Modulator Fabrication & Characterization

5.1 Silicon electro-optic modulator fabrication

The fabrication process includes three major steps, namely a) waveguide fabrication, b) ITO fabrication and c) Al contact fabrication. An n-type doped SOI wafer (Fig.5.1) with a doping concentration of 1×10^{17} cm^{-3} is used, in accordance with the considerations discussed in chapter 2. The SOI wafer was cleaved and cleaned in hot trichloroethylene, acetone and isopropyl alcohol (IPA) using a sonic bath, followed by cleaning in hot aqua regia solution for 10 minutes to remove metal contaminations, followed by rinsing in DI water. Finally, the sample is soaked in the piranha solution for 10 minutes to remove polymer contaminations.

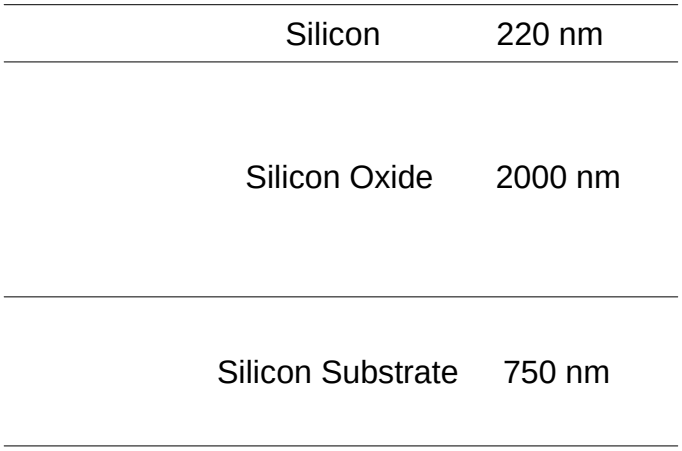


Fig.5.1 SOI wafer structure. The numbers are the thickness of each layer. The top silicon layer is n-type doped (1×10^{17} cm^{-3}).

After all these cleaning steps, the sample is ready for resist coating. ZEP 520A is used as the electron-beam resist, spun at 3750 rpm for 1 minute, resulting in a thickness of 400 nm. After spin coating, the sample is baked at 180˚C for 10 minute in air to dry off the solvent. Then, the sample is ready for electron beam writing. Following electron beam exposure, the sample is developed in Xylene at 23˚C for 1 minute and 45 seconds. Then, the sample is rinsed in IPA. As ZEP 520A is a positive photoresist, the region exposed to the electron beam dissolves in the developer. After development, the sample is etched using reactive-ion etching (RIE) to form the optical structure. Fig.5.2 shows the process of the waveguide fabrication.

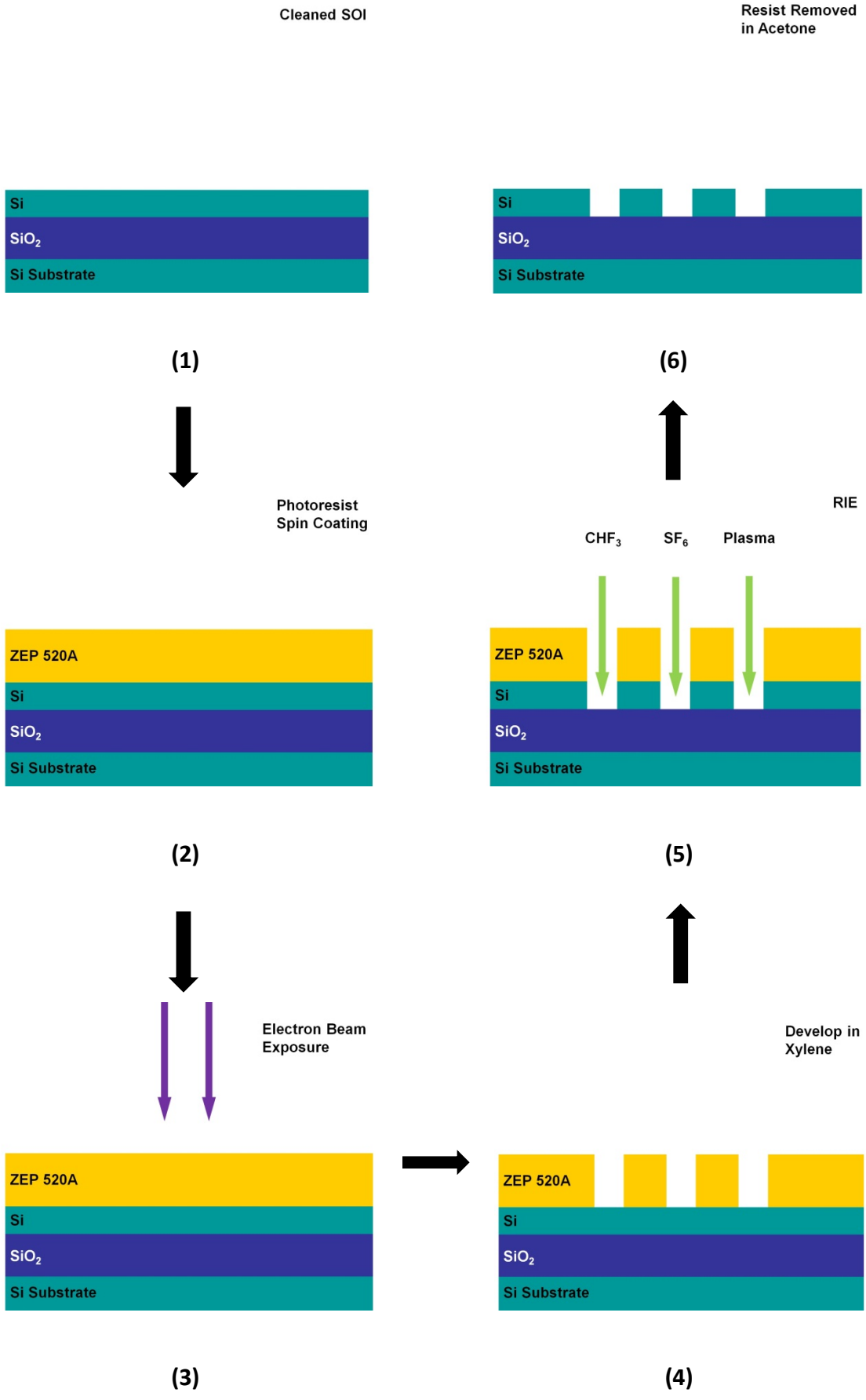
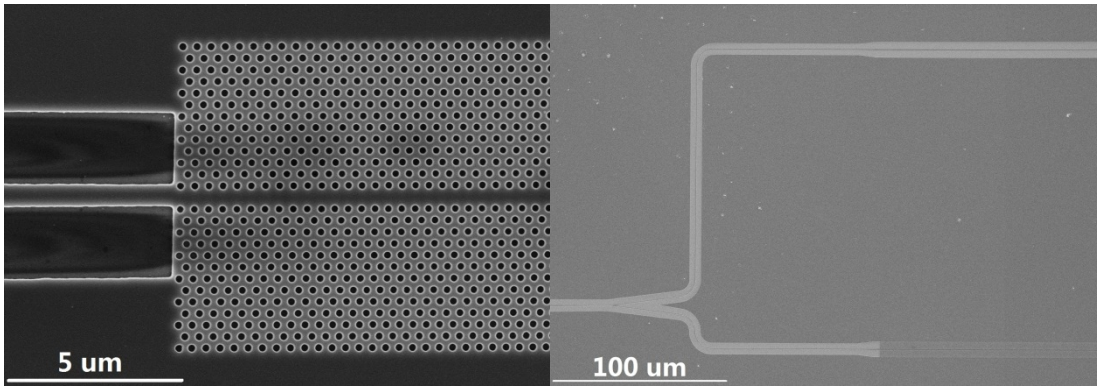

Cleaned SOI
Si
SiO_2
Si Substrate
(1)
Photoresist
Spin Coating
ZEP 520A
Si
SiO_2
Si Substrate
(2)
Electron Beam
Exposure
ZEP 520A
Si
SiO_2
Si Substrate
(3)
Develop in
Xylene
ZEP 520A
Si
SiO_2
Si Substrate
(4)
RIE
CHF_3
SF_6
Plasma
ZEP 520A
Si
SiO_2
Si Substrate
(5)
Resist Removed
in Acetone
Si
SiO_2
Si Substrate
(6)

Fig.5.2 Silicon photonic crystal fabrication process

(1) Cleaned SOI wafer; (2) Spin coat electron beam photoresist – ZEP 520A; (3) Electron beam exposure; (4) Develop in Xylene. The exposed ZEP 520A dissolves in the developer; (5) RIE in CHF_3 and SF_6; (6) Resist residual is removed in acetone.

The RIE process is a chemical assisted plasma etch. The chemicals used for etching silicon are CHF_3 and SF_6. The process is very sensitive to contamination from other gases, so the chamber is always cleaned using a sequence of H_2, Ar and O_2 plasma. The RIE chamber is pumped down until the pressure drops below 3×10^{-6} mbar to remove air and water vapour. Following pump-down, preconditioning step is performed with CHF_3 and SF_6 at pressure of 5.9×10^{-2} mbar for 10 minutes. Then, the sample is etched at a power of 21 W for 1 minute 50 seconds. After the RIE, the sample is cleaned in 1165 solution, followed by acetone and IPA using a sonic bath to remove ZEP residual. Fig.5.3 shows a typical structure after RIE etch, including photonic wires, PhC waveguides and Y-junctions.



(a) **(b)**

Fig.5.3 SEM picture of optical structures after RIE. (a) shows slow light engineered PhC waveguides with a taper on the left. (b) shows half of a MZI structure with a Y-junction and PhC waveguides.

Although the optical loss of ITO is much smaller than that of metal, ITO still has a relatively large optical absorption (see chapter 3). Therefore, a thin FOx layer is used as a spacer between the silicon waveguides and the ITO. The diluted FOx (FOx 14 : MIBK = 1 :2) is spun at 7000 rpm on the sample for 1 minute. Then, the sample is baked at 100˚C for 10 minutes, followed by 200˚C for 15 minutes. The temperature is raised by 50˚C every 15 minutes up to 400˚C and then kept at 400˚C for 4 hours. After that, the sample cools down naturally. The resulting FOx thickness is around 70 ~ 80 nm.

The next step is to open windows on the photoresist for ITO deposition. Fig.5.4 shows the process of ITO deposition and lift-off. In order to achieve high resolution, electron beam lithography is used to open ITO windows with PMMA rather than ZEP 520A as electron beam resist, as ZEP 520A needs an extra bottom resist layer such as lift-off resist LOR 7B, to create undercuts for lift-off. Diluted

PMMA 950K (PMMA 950K : Thinner = 2 : 1) is spun at 1500 rpm for 1 minute and baked at 180˚C for 10 minutes. For a successful lift-off, the resist must be at least twice as thick as the deposited film. Here, the PMMA thickness is around 440 nm which is enough for 200 nm Al lift-off. As ITO windows must be precisely opened on the correct position, 3 point alignment is used. Following exposure, the sample is developed in IPA : DI water = 7 : 3 for 1 minute 45 seconds. It is then rinsed in pure IPA for over 1 minute to stop the development. After that, the sample is loaded into the electron beam evaporator for ITO deposition.

The ITO is deposited at an incident angle of 45˚. The rate is kept at around 0.01 nm/s and never higher than 0.03 nm/s. 140 nm ITO is typically deposited. After deposition, the sample is soaked in acetone to perform lift-off. Then, the sample is annealed at 400˚C for 30 minutes. The annealing also hardens the ITO film. Finally, the sample is cleaned in acetone and IPA using a sonic bath.

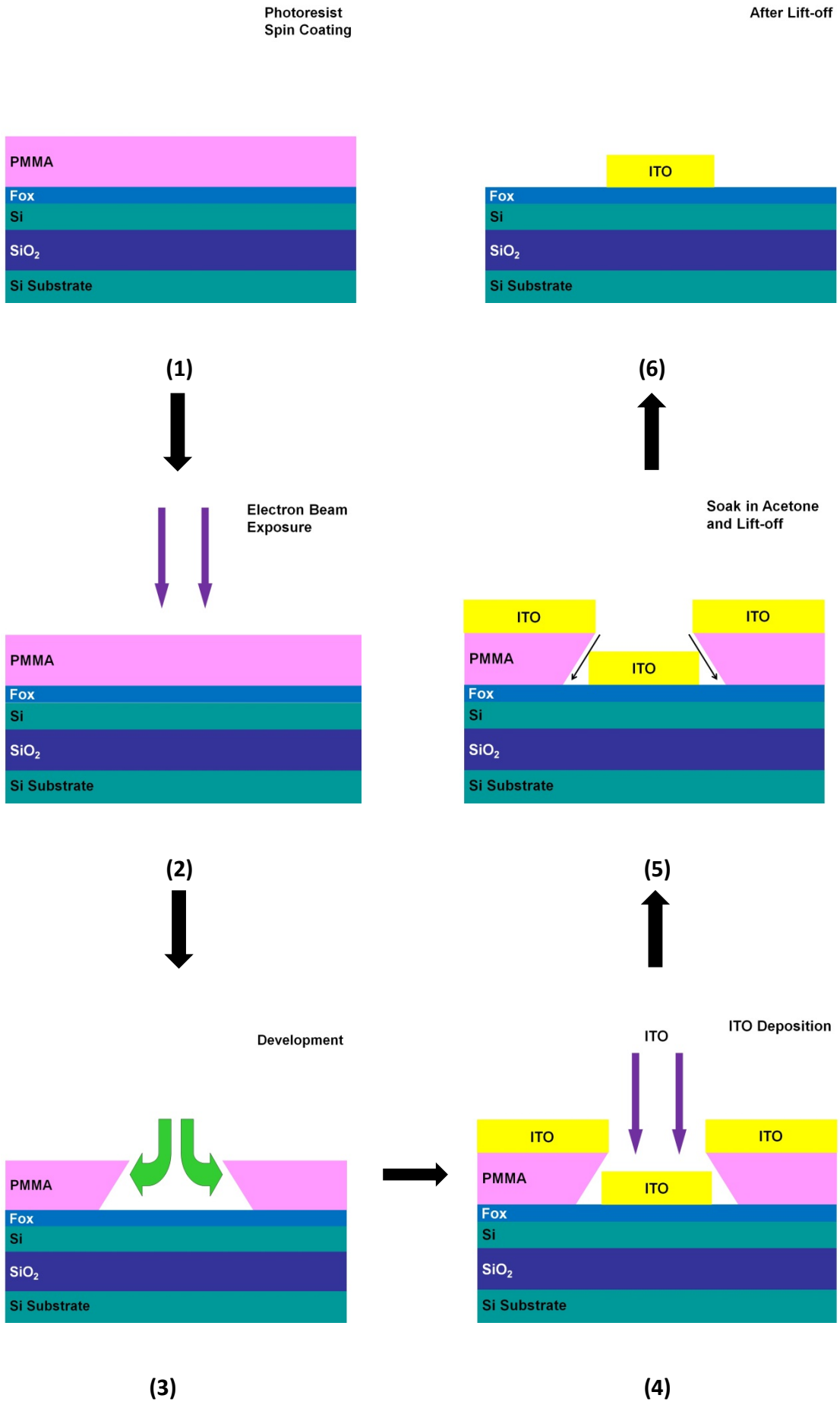

Photoresist
Spin Coating
PMMA
Fox
Si
SiO_2
Si Substrate
(1)
Electron Beam
Exposure
PMMA
Fox
Si
SiO_2
Si Substrate
(2)
Development
PMMA
Fox
Si
SiO_2
Si Substrate
(3)
ITO
ITO
ITO
PMMA
Fox
Si
SiO_2
Si Substrate
(4)
Soak in Acetone
and Lift-off
ITO
ITO
ITO
PMMA
Fox
Si
SiO_2
Si Substrate
(5)
After Lift-off
ITO
Fox
Si
SiO_2
Si Substrate
(6)
ITO Deposition

Fig.5.4 ITO deposition and lift-off process

(1) Spin coat electron beam photoresist – PMMA; (2) Electron beam exposure; (3) Development; (4) ITO deposition; (5) Soak in acetone. The acetone flows into the undercut and lift off the resist and unwanted ITO; (6) ITO contact after lift-off.

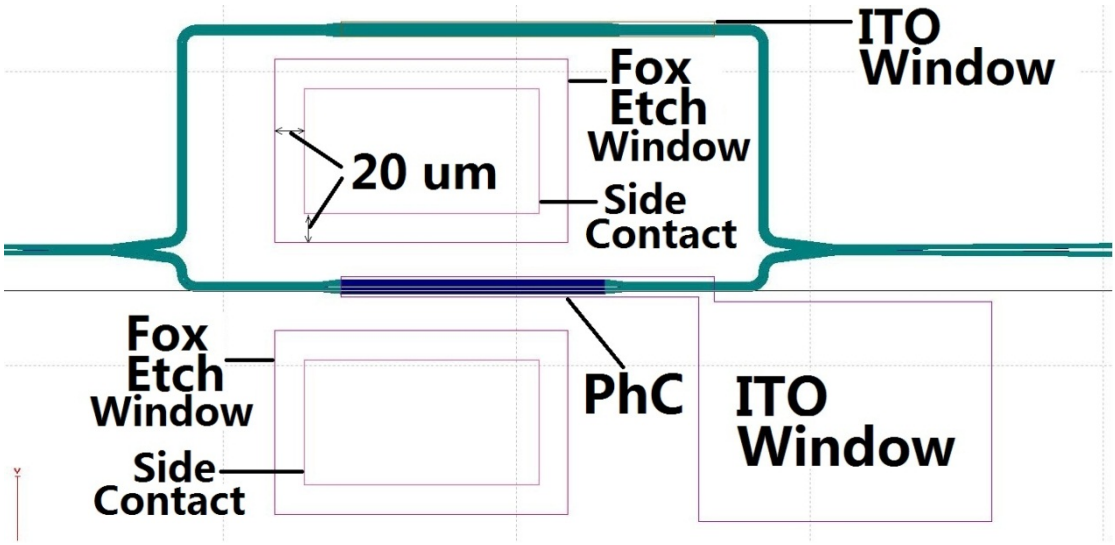


Fig.5.5 GDS design structure of an asymmetric MZI. It shows the layout of all the components of the modulator. The blue area is the PhC waveguide with an ITO window on top. The FOx etch window is 20 um larger than the Al contact window as it is easier to align the structures under the microscope with a large spacing between each other.

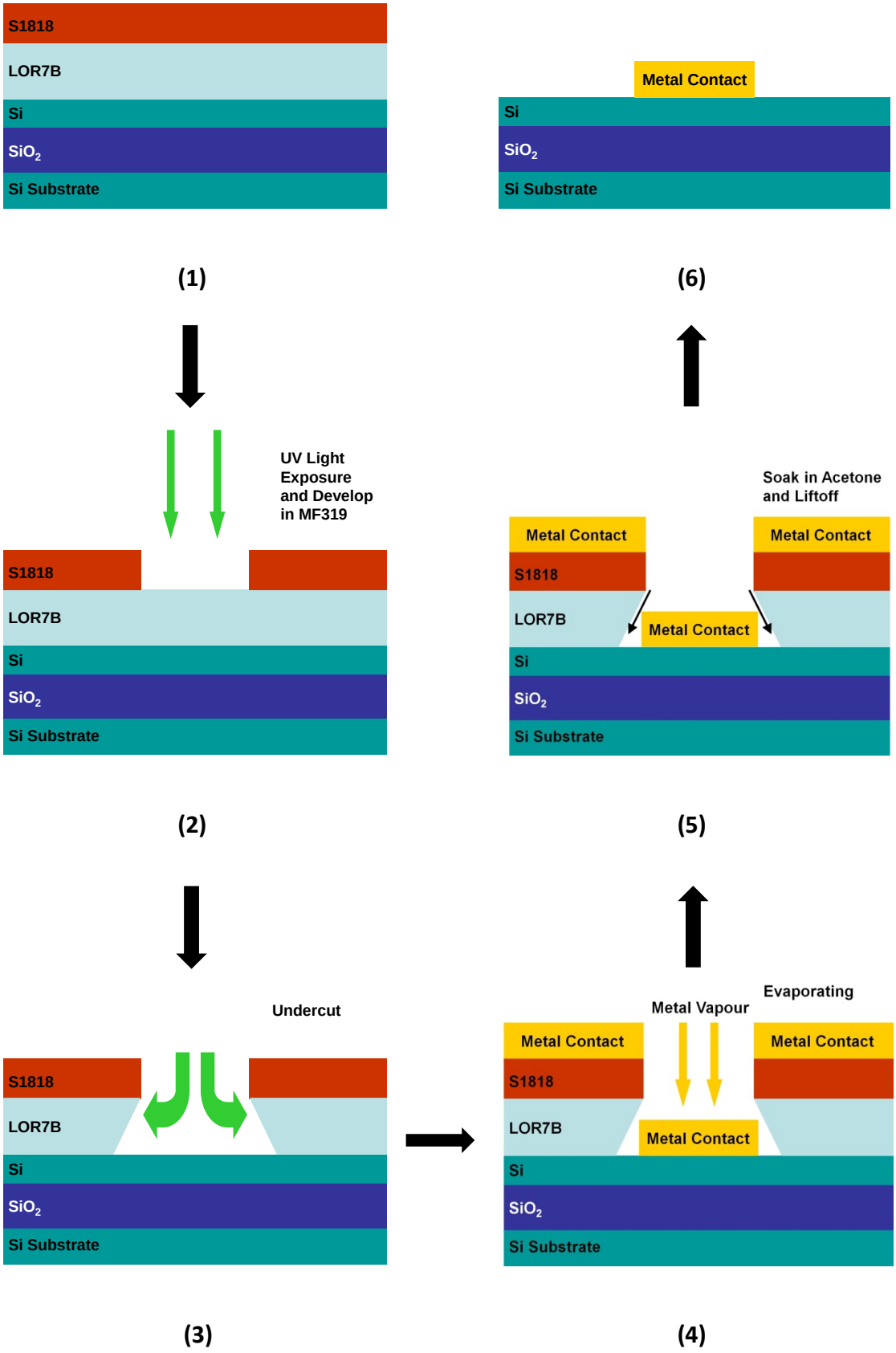


Fig.5.6 Metal contact lift-off process

(1) Photoresist (S1818) and lift-off resist (LOR 7B) coating. S1818 is around 2 um thick and LOR 7B is about 700 nm thick. (2) UV light exposure using a photomask with Al contact window. Then the sample is developed in MF319; (3) MF319 forms undercuts in LOR7B; (4) Metal (Al) deposition; (5) Soak the sample in acetone. The acetone flows into the undercut and lift off the resist and unwanted metal (Al); (6) Metal (Al) contact after lift-off.

The final step is Al contact fabrication. As the entire sample is coated by FOx, it must be etched prior to Al deposition. The FOx etch window is opened by photolithography with S1818 G2 as photoresist. S1818 G2 is spun at 5000 rpm for 1 minute and baked at 100˚C for 1 minute. The high resolution UV exposure is performed in the automated mask alignment system EVG 620. The sample is developed in MF319 for 40 seconds and rinsed in DI water. The FOx etch window is made 20 um larger than the Al contact window, so that it is easier to align the structures under the microscope (see Fig.5.5). The sample is then etched in the RIE by CHF_3 assisted plasma for 10 minutes to remove the FOx unprotected by S1818. The etch pressure is 4×10^{-2} mbar and the power is 41 W. This RIE etch is quite selective; the SiO_2 etch rate is around 25 nm per minute while the silicon etch rate is only 0.1 nm/min. Following RIE, the sample is cleaned in 1165 solution, acetone and IPA using a sonic bath to remove any S1818 residual. The sample is then ready to pattern the Al contact windows.

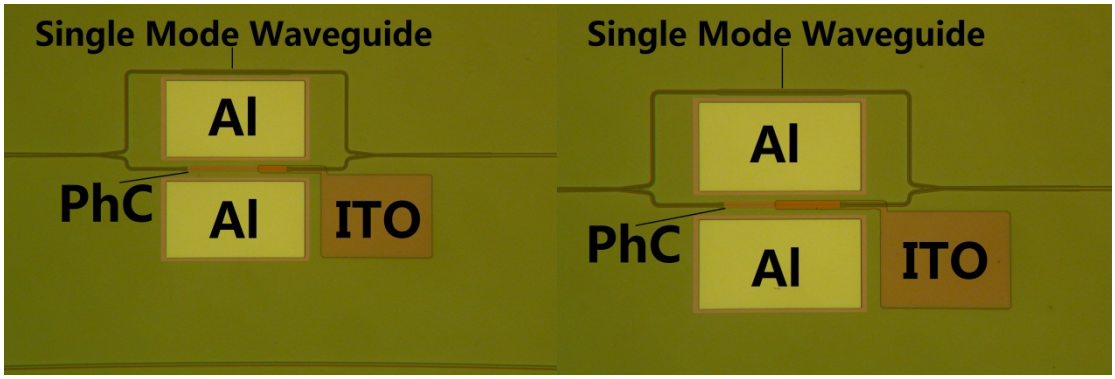
The Al contact fabrication process is shown in Fig.5.6. The lift-off resist LOR 7B is used in Al contact fabrication, which forms an undercut in MF319, below the exposed S1818 region. LOR 7B is spun at 4000 rpm for 1 minute and baked at 180˚C

for 5 minutes. Then, S1818 G2 is spun at 5000 rpm for 1 minute and baked at 100˚C for 1 minute. So there are 2 layers of resists (S1818 and LOR 7B) on the sample. Then, the Al contact window is opened by photolithography. UV exposure and development is the same as mentioned above. After development, the sample is loaded into a thermal evaporator for Al deposition. Al deposition is carried out with a rate of around 0.2 nm/s, aiming for a final thickness of 200 nm. Following deposition, excess Al and resists are removed by lift-off. Finally, the sample is ready for cleaving and optical testing.

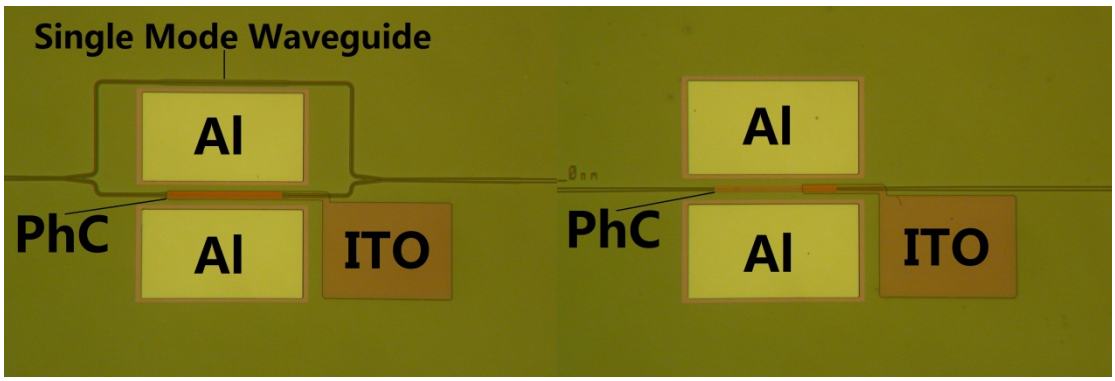
5.2 Silicon electro-optic modulator optical transmission characterization

5.2.1 Asymmetric MZI modulator with ITO on one arm

The first silicon electro-optic modulator was fabricated with ITO on the phase shifter arm of only one arm of an asymmetric MZI structure. The reason for choosing an asymmetric MZI instead of a symmetric MZI is that an asymmetric MZI is more sensitive to refractive index changes than a symmetric one, if operated in the “critical coupling” regime. Furthermore, the output intensity of an asymmetric MZI is a function of the wavelength. Therefore, it is easier to observe phase changes from an asymmetric MZI.



(a) Modulator with 50 um ITO on PhC (b) Modulator with 100 um ITO on PhC



(c) Modulator with 180 um ITO on PhC (d) Phase Shifter with 50 um ITO on PhC

Fig.5.7 Asymmetric MZI silicon electro-optic modulators with ITO only on one arm. The FOx thickness is 70 - 80 nm and appears dark brown in the pictures. The ITO layer is 140 nm thick and is only on the phase shifter arm. The light brown area around the Al contact is the FOx etch window, which is slightly bigger than the Al contact window. A single mode waveguide is in the reference arm, while the PhC waveguide is in the phase shifter arm. (a) Modulator with ITO length 50 um; (b) Modulator with ITO length 100 um; (c) Modulator with ITO length 180 um; (d) Phase Shifter with ITO length 50 um. These are the devices that I fabricated and measured.

Considering the ease of fabrication and testing, an active phase shifter length of 180 um is chosen as a suitable starting point. The phase-intensity modulation can still be observed from the modulator with this phase shifter length. Once the simplified device works, the full size modulator will be fabricated and tested.

Three different lengths of ITO were fabricated on the 180 um long photonic crystal waveguide, namely 50 um, 100 um and 180 um, in addition to a 75 um long strip of ITO on the silicon waveguide, so the total ITO lengths are 125 um, 175 um and 255 um. We used slow light engineered PhC waveguides with a hole diameter of 180 nm and a period of 400 nm (PhC400). Other PhC waveguides with periods of 390 nm (PhC390) and 410 nm (PhC410) were also fabricated, to account for fabrication tolerances. A FOx layer (70 - 80 nm thickness) was added to separate the ITO from the waveguide. A typical layout is shown in Fig.5.7.

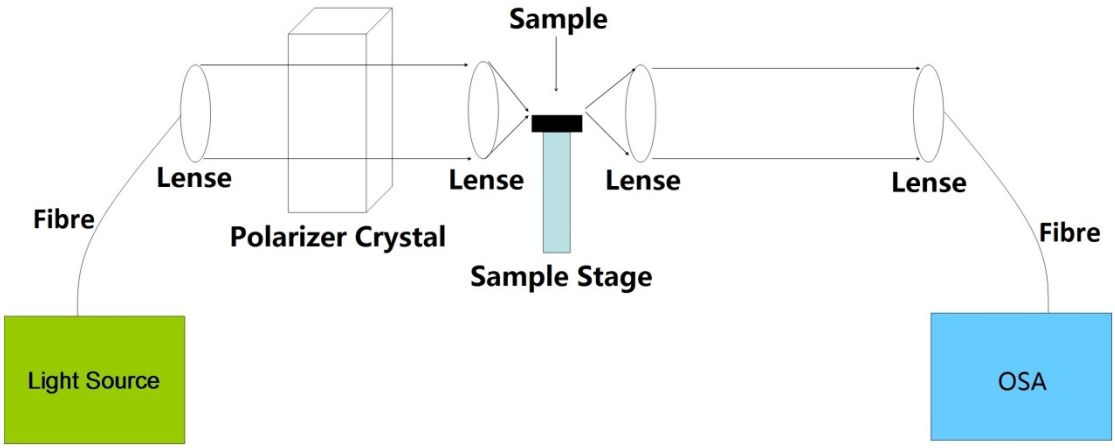


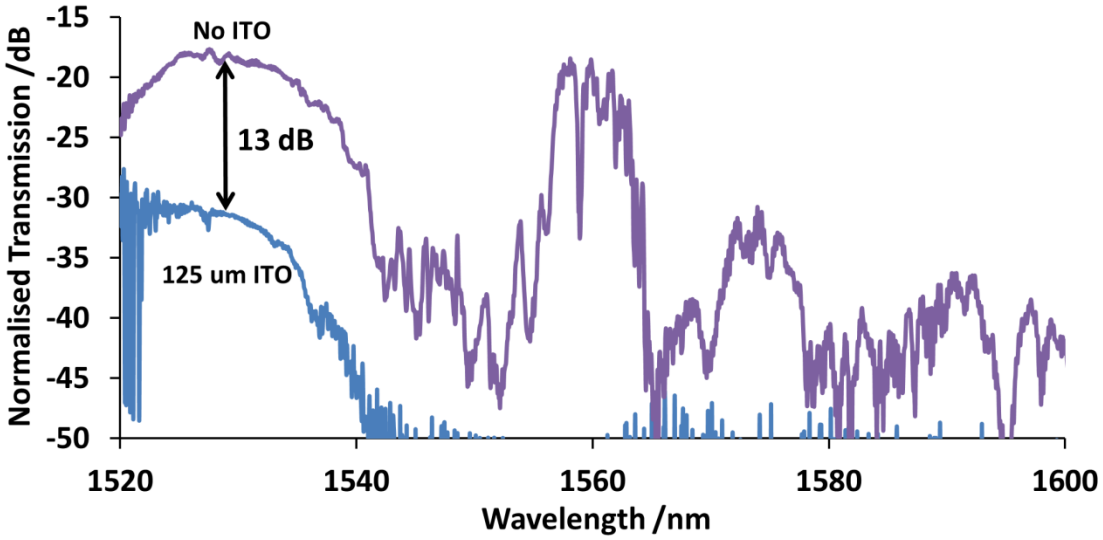
Fig.5.8 Optical transmission spectrum measurement system. The light source used is an ASE source (Amonics C+L Band ASE Source) and the optical spectrum analyser (OSA) used is an Advantest Q8384. Only the TE polarization is loaded to the sample.

Optical transmission was measured on the setup shown in Fig.5.8. A polarizer ensures that only TE polarisation is launched into the sample. The light source used is an ASE source (Amonics C+L Band ASE Source) and the optical spectrum analyser (OSA) used is an Advantest Q8384.

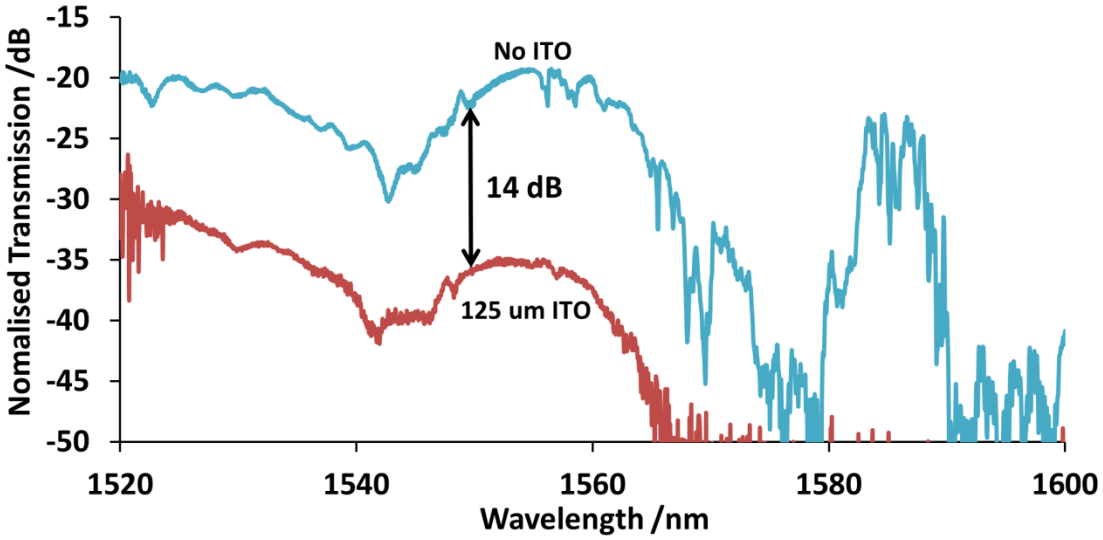
The ASE source is driven at maximum output power 52 mW. The OSA scanning wavelength is 1520 nm ~ 1600 nm and the resolution is 0.1 nm. The OSA is controlled by a computer program to scan and collect transmission data. The measured transmission spectra are normalised to the ASE source otherwise specified.

5.2.1.1 Absorption due to ITO

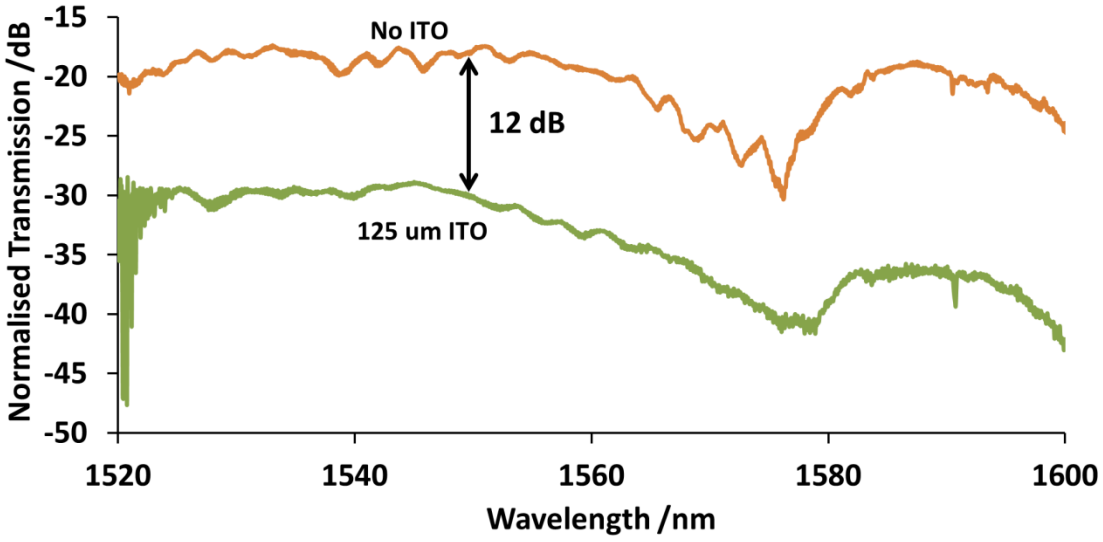
Before assessing the MZI samples, the transmission of straight PhC waveguides with and without ITO were measured. The ITO covered 50 um length on the PhC and 75 um on the access waveguide. The corresponding transmission for different PhC periods is shown in Fig.5.9, comparing transmission with and without ITO coating. For all three PhC waveguides with different periods, loss due to 125 um long ITO is over 10 dB which is higher than previous ITO loss test results in chapter 3 where the loss was 7 ~ 8 dB. The higher loss here is probably due to the fact that the evanescent tail of a photonic crystal waveguide mode extends further into the cladding, therefore interacts more strongly with the lossy ITO.



(a) Normalised transmission spectra of PhC390 with and without 125 um long ITO



(b) Normalised transmission spectra of PhC400 with and without 125 um long ITO

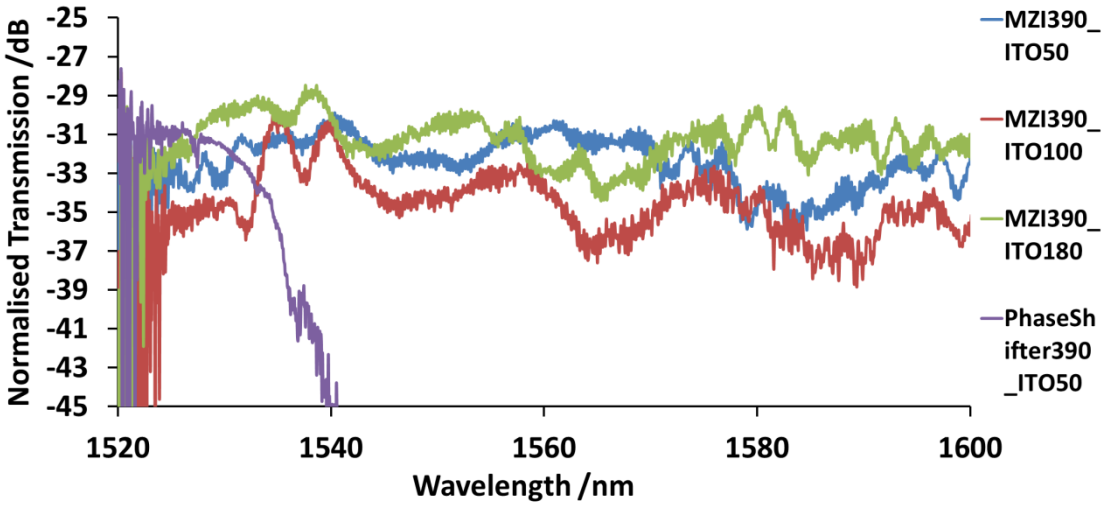


(c) Normalised transmission spectra of PhC410 with and without 125 um long ITO

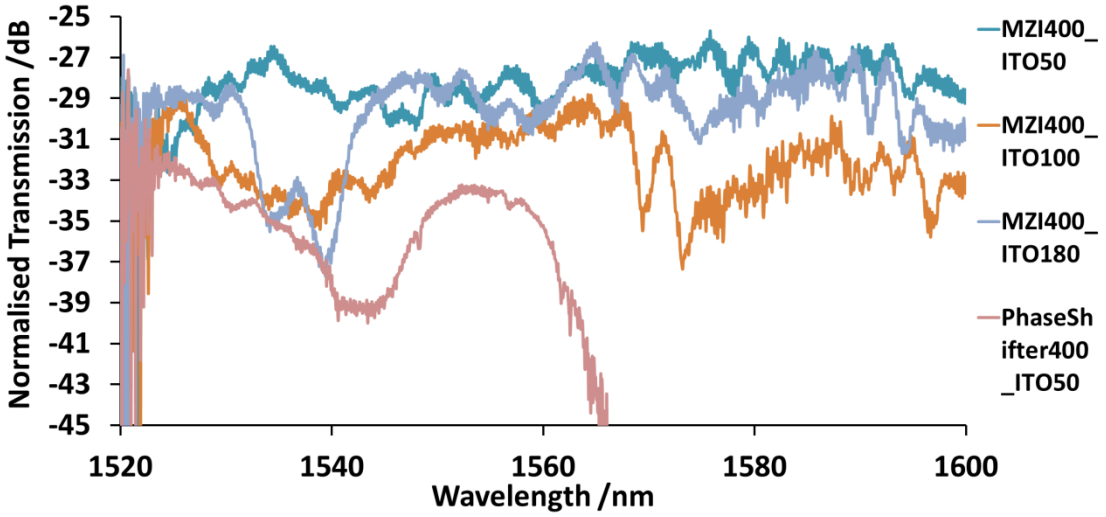
Fig.5.9 Normalised transmission spectra of PhC waveguides with and without 125 um long ITO. The loss due to 125 um long ITO is over 10 dB depending on wavelength. The long-wavelength cut-off scales with the lattice period, as expected, and is positioned at λ≈1540 nm for a=390 nm period, λ≈1565 nm for a=400 nm and λ>1600 nm for a=410 nm.

5.2.1.2 Transmission measurement of MZI modulator without applied voltage

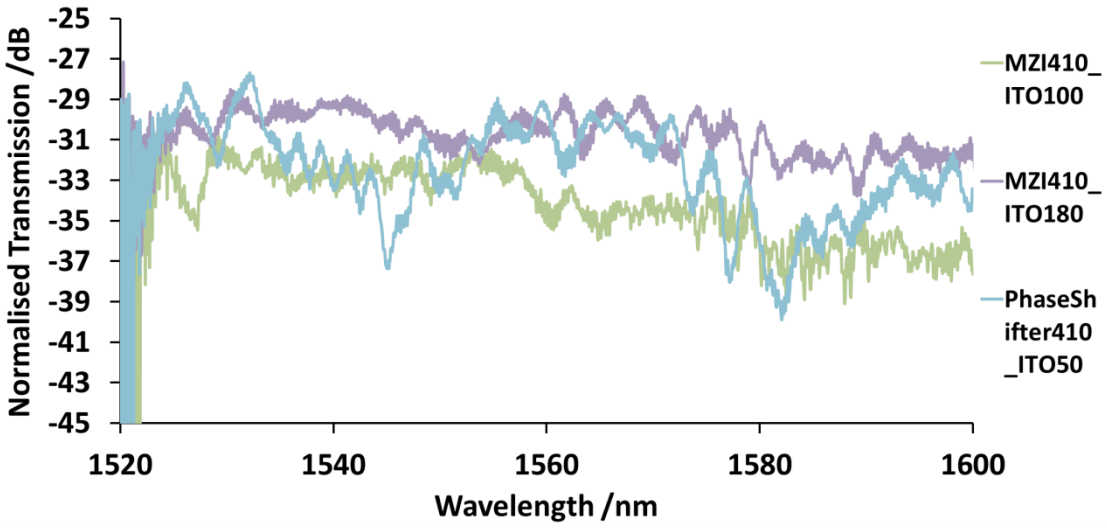
Following this initial investigation, the optical transmission of the MZI modulators with different PhC periods and different ITO lengths were measured. At this point, no voltage is applied to the contacts. Fig.5.10 shows the normalised transmission spectra of MZI modulators and also the transmission spectra of phase shifters for each period of PhC waveguides as references.



(a) Normalised transmission spectra of PhC390 MZI modulator and PhC390 phase shifter. The cutoff of the phase shifter at 1540 nm indicates that the output of MZI modulator is mainly from the reference arm. The ITO films are only on the phase shifter arms of the MZI modulators.



(b) Normalised transmission spectra of PhC400 MZI modulator and PhC400 phase shifter.



(c) Normalised transmission spectra of PhC410 MZI modulator and PhC410 phase shifter.

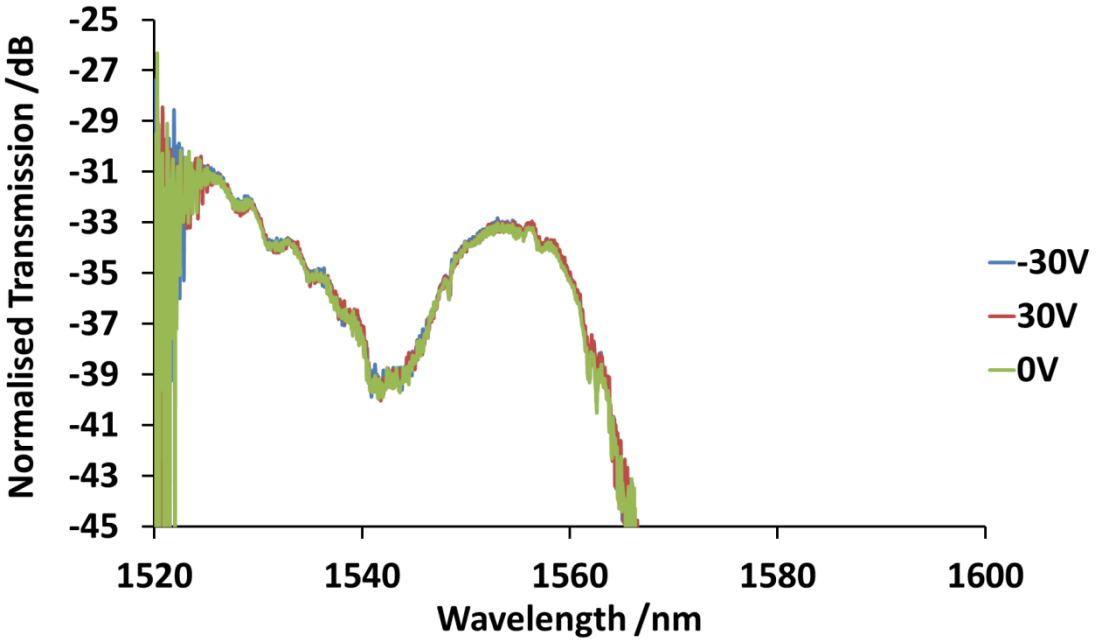
Fig.5.10 Normalised transmission spectra of MZI modulators and phase shifters. The measured devices are shown in Fig.5.7. The ITO films are only in the phase shifter arms of the MZI modulators.

Transmission spectra of the phase shifters shown in Fig.5.10 help to find the MZI interference pattern. Because light through the phase shifter has been cut off at the PhC cutoff wavelength, no interference is observed beyond the cutoff wavelength; this is particularly noticeable for the a=390 nm sample, where transmission through the phase shifter is cut off beyond λ=1540 nm. Thus, for longer wavelengths, the transmission is solely determined by the reference arm. It is clear that transmission through the MZI is dominated by the reference arms and that no distinct interference pattern is visible. We believe that this is due to the fact that light through the reference arm is much stronger than light through the phase shifter arm, considering that transmission of the phase shifters is much lower than that of

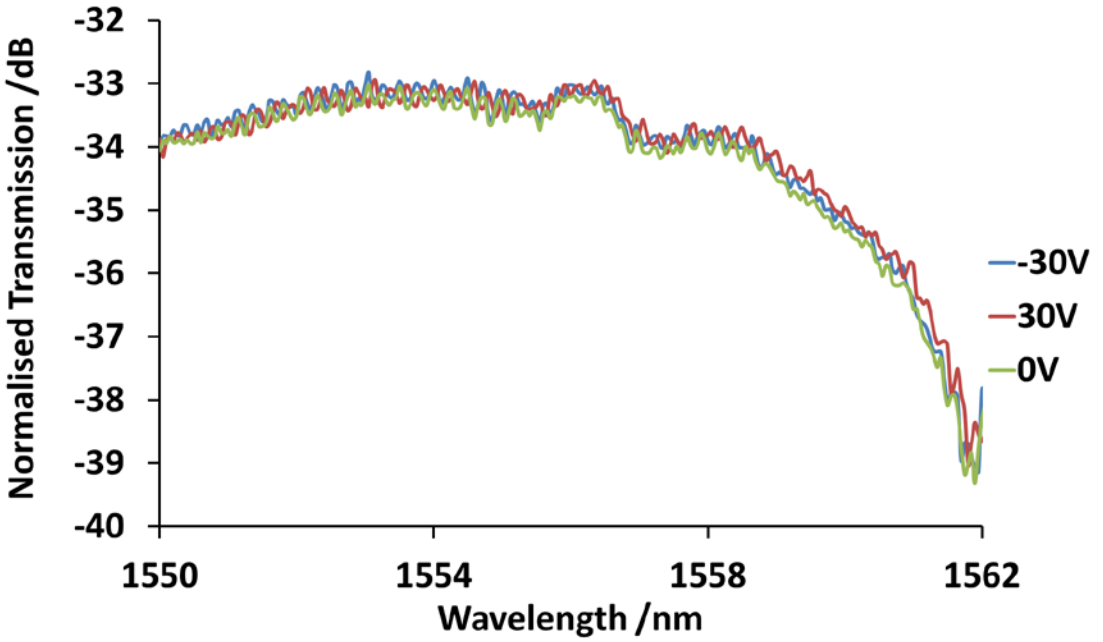
the MZI modulators. Therefore, the interference between light from the two arms is too weak to see.

5.2.1.3 Transmission measurement of phase shifters with applied voltage

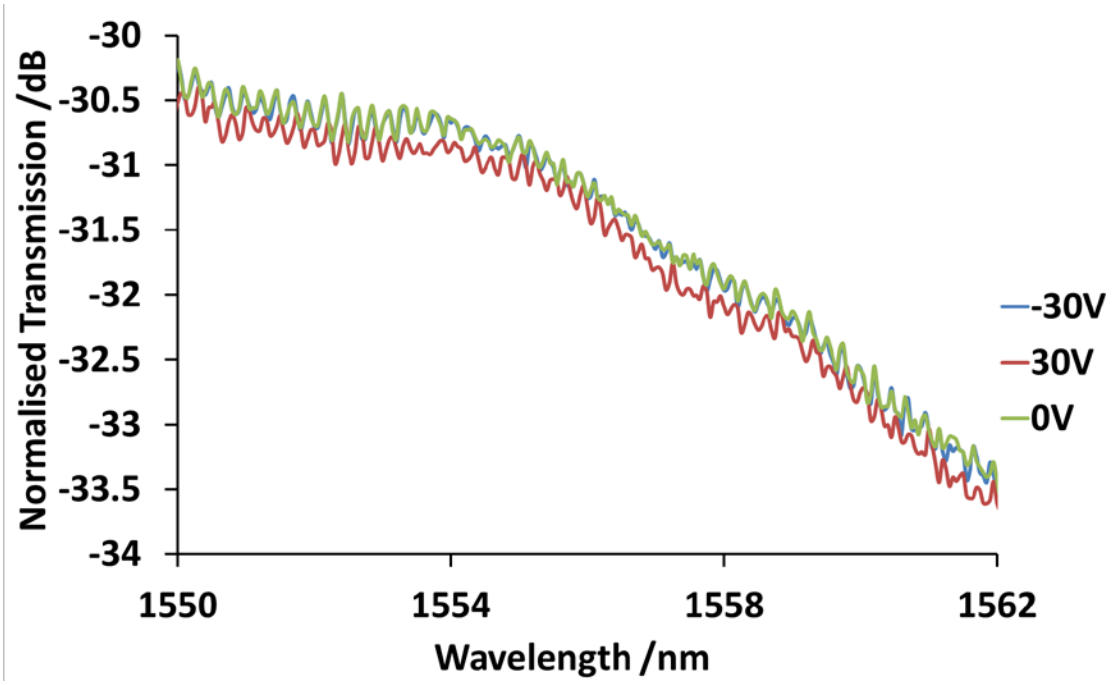
In order to test the electro-optic properties of the phase shifters, we applied a Voltage to the a=400 nm sample. Fig.5.11 shows the corresponding transmission vs. Voltage plot. The voltages applied to the ITO central contact are -30 V, 0 V and +30 V. The two side contacts are grounded.



(a) Normalised transmission spectra (1520-1600 nm) of PhC400 phase shifter (50 um ITO) at applied voltages.



(b) Normalised transmission spectra in a smaller wavelength range (1550-1562 nm) of PhC400 phase shifter (50 um ITO) at applied voltages.



(c) Normalised transmission spectra in a smaller wavelength range (1550-1562 nm) of PhC410 phase shifter (50 um ITO) at applied voltages.

Fig.5.11 Normalised transmission spectra of PhC400 & PhC410 phase shifters (50 um ITO) at applied voltages. (b) is the magnified view of (a), which focuses on the wavelength from 1550 nm to 1562 nm. (c) shows that the transmission spectra pattern has very weak loss change and shift at applied voltages.

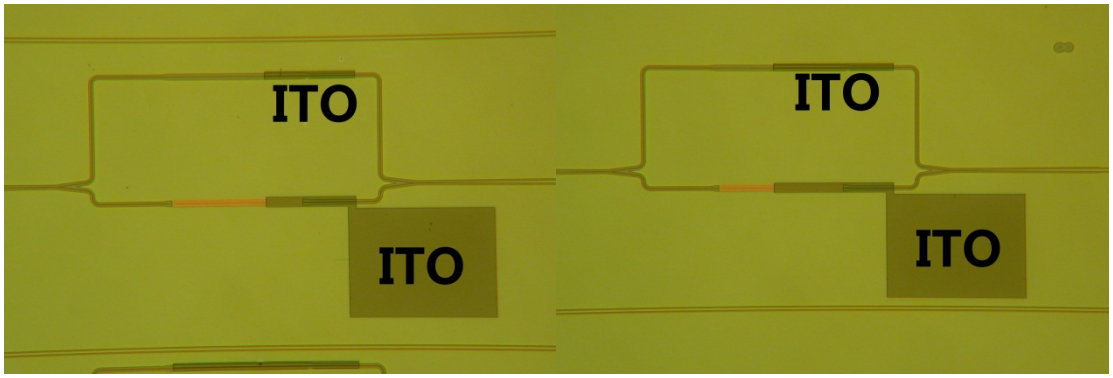
We expect that by applying a negative voltage on the ITO central contact, electrons in the n-type silicon under the ITO are depleted and the depletion region occurs. Hence, the carrier concentration in phase shifter waveguide reduces. As a result, optical loss becomes smaller and transmission increases. Contrarily, by applying a positive voltage, the loss should increase (transmission should drop). From Fig.5.11 (a), however, it is difficult to see any loss change between the transmission spectra, even though, magnifying Fig.5.11 (a) into a small wavelength range (Fig.5.11 (b)). Nevertheless, for the PhC410 phase shifter with 50 um long ITO, the magnified transmission spectra from 1550 nm to 1562 nm (Fig.5.11 (c)) shows that the transmission at -30 V and 0 V is slightly higher than that at +30 V. This agrees with our expectation, as the negative Voltage should create a depletion layer, hence lower loss. Since the loss change is so weak, the carrier density change is very small. One possible reason could be that the ITO is not conductive enough and a considerable fraction of the electric field already drops across the ITO. Nevertheless, we proceeded to building an MZI with ITO on both arms, with expectation that the phase change should be visible when both arms are equally lossy; also, we expect the phase change to be more sensitive in an interferometric device than the amplitude change in a simple waveguide.

5.2.2 Asymmetric MZI modulator with ITO on both arms.

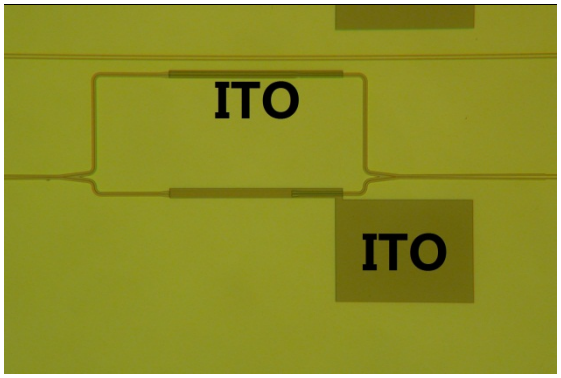
In order to balance optical power in the two arms, another sample was fabricated with almost the same design as before, but the same length of ITO on both arms. To ensure that the modulators have a clear MZI interference pattern, the sample was cleaved after ITO fabrication and the transmission was initially measured before Al contact deposition. In a second step, Al contacts were deposited and the transmission was measured again.

5.2.2.1 Transmission measurement before FOx etching and Al contact fabrication

We were finally able to observe an MZI interference pattern on these balanced modulators. First, the devices are shown in Fig.5.12.

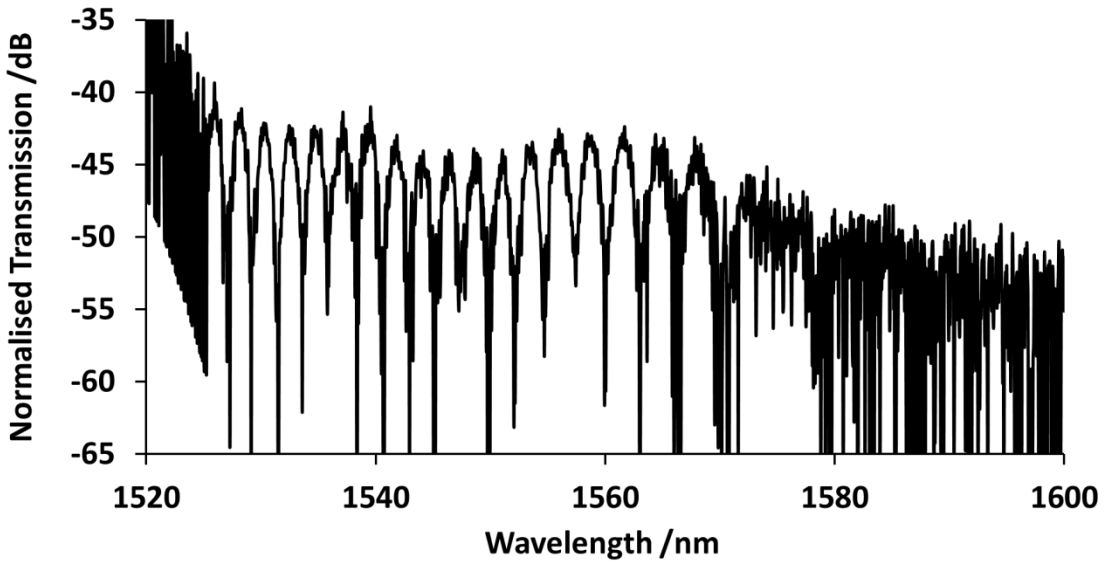


(a) Modulator with 50 um ITO **(b) Modulator with 100 um ITO**

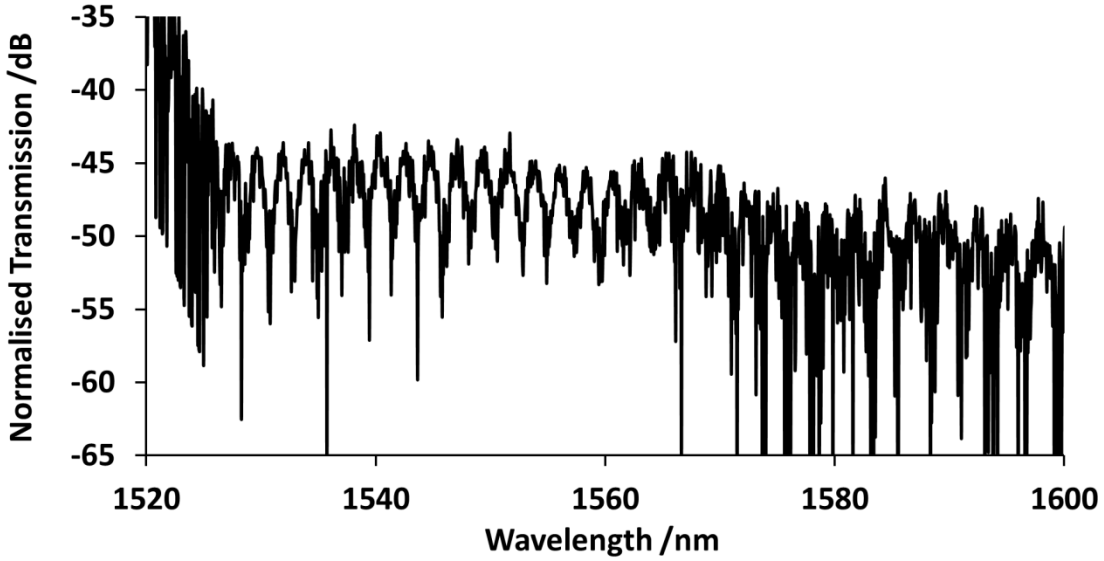


(c) Modulator with 180 um ITO

Fig.5.12 Top view of fabricated modulators before Al contact deposition. The ITO deposited on the reference arm is of the same length as that on the phase shifter arm.



(a) Normalised transmission spectrum of PhC400 MZI modulator with 50 um ITO



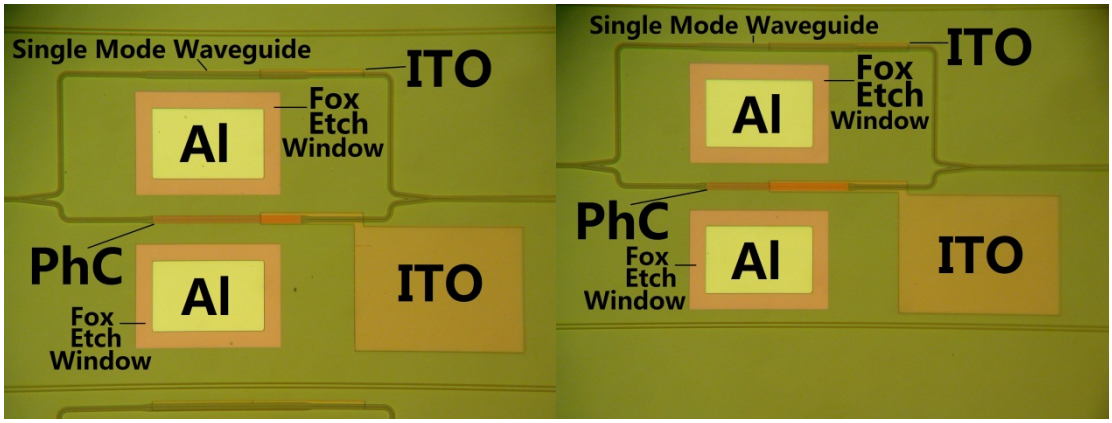
(b) Normalised transmission spectrum of PhC410 MZI modulator with 100 um ITO

Fig.5.13 Normalised transmission spectra with MZI interference pattern. The transmission spectra show the MZI interference pattern of devices in Fig.5.12. The ITO films are on both arms of the MZI structures.

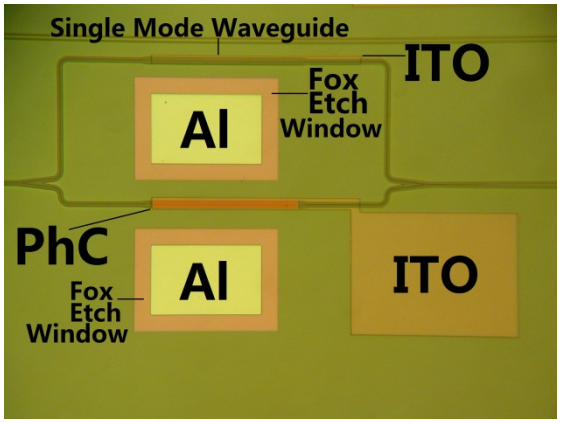
Although the two modulators in Fig.5.13 clearly show an MZI interference pattern, the optical power is very low, which makes transmission measurement very difficult. The peak-to-peak fringe spacing which is determined by wavelength and also the difference of the optical path between the two arms is 2.2 - 2.5 nm. Correspondingly, the output of devices with 180 um long ITO was too weak to measure in the OSA.

5.2.2.2 Transmission measurement after FOx etching and Al contact fabrication

Once the MZI interference pattern was observed, the fabrication continued with FOx etching and Al contact deposition. The finished devices are shown in Fig.5.14. As the sample had already been cleaved and the alignment marks for photolithography had been cleaved off, the FOx etching window and Al contact window were opened in the electron beam machine using photonic crystal for alignment.



(a) Modulator with 50 um ITO **(b) Modulator with 100 um ITO**



(c) Modulator with 180 um ITO

Fig.5.14 Microscope view of fabricated modulators after FOx etching and Al contact fabrication. The ITO deposited on the reference arm is the same length as that on the phase shifter arm.

Following Al contact fabrication, the transmission of the MZI modulators was too weak to measure. Even though the fibre splitter was removed and an erbium-doped fibre amplifier (EDFA) was used to amplify the output light, the optical signal was still too weak to detect.

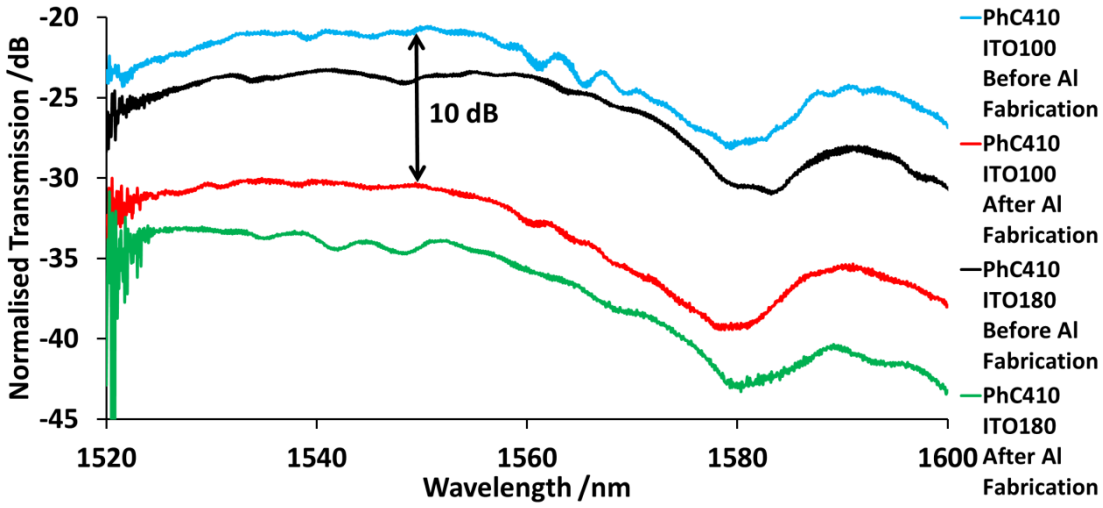
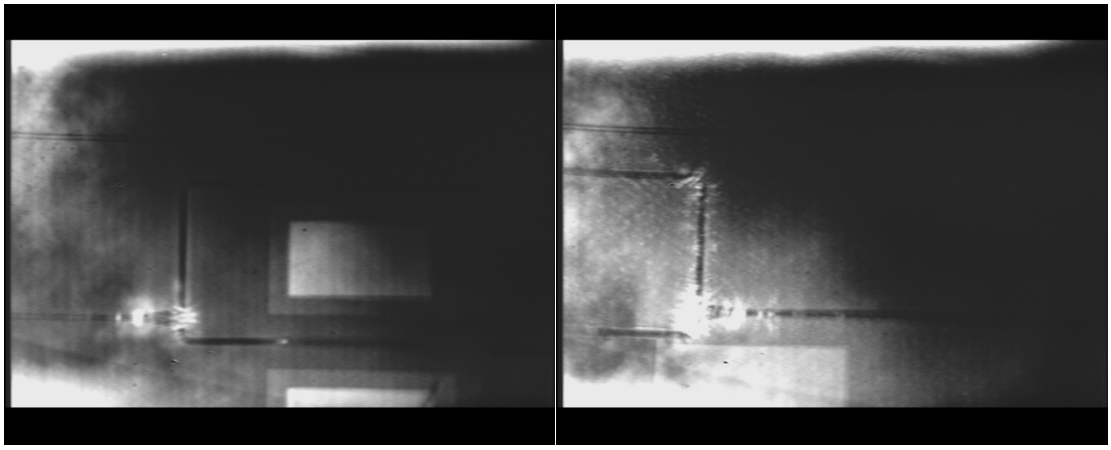


Fig.5.15 Individual PhC waveguides (PhC410) transmission spectra before and after FOx etching and Al contact deposition. The transmission difference shows the loss due to the FOx etching and Al contact deposition.

Although it was impossible to measure the transmission of the complete MZI devices, the individual photonic crystal waveguides (PhC410) transmission shows the difference before and after FOx etching and Al contact fabrication (see Fig.5.15). Optical loss between different PhC400 waveguides is over 8 dB, while loss between different PhC410 waveguides is around 10 dB for ITO50 and more than 10 dB for ITO180. These losses must be due to Al contact deposition.

Strong scattering light can be seen at the Y-junction and bent waveguides, which is shown in Fig.5.16. This scattering might explain the high losses.

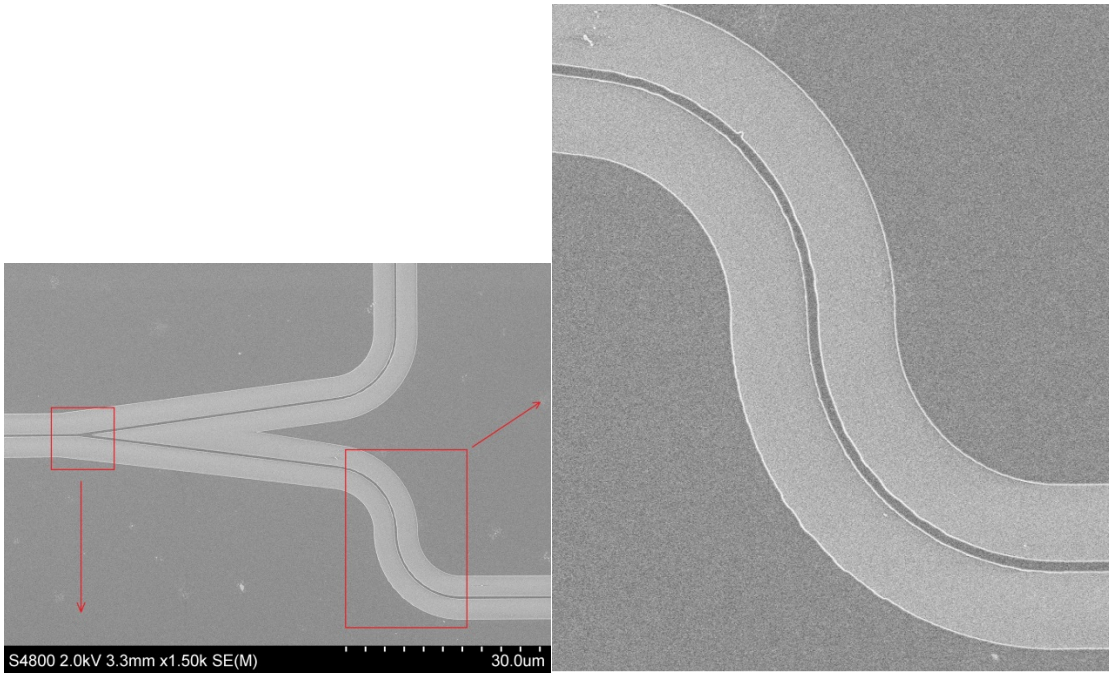


(a) **(b)**

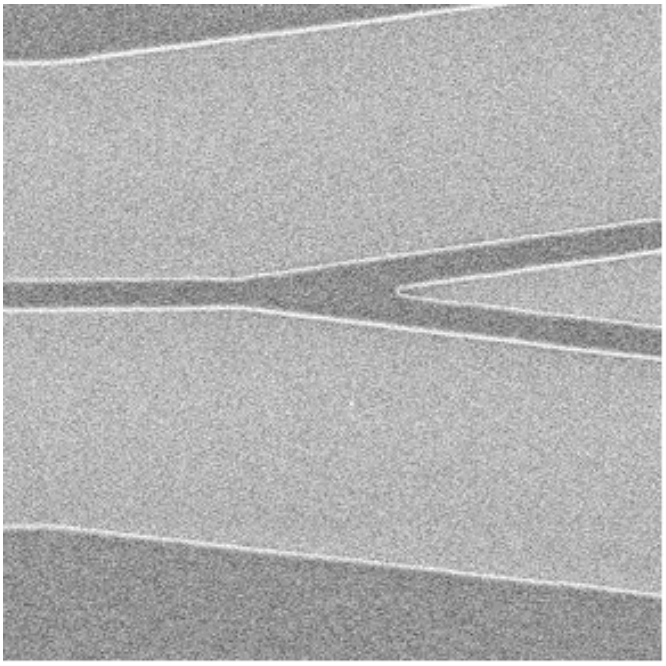
Fig.5.16 Microscope view of a MZI modulator with strong scattering at Y-junctions and waveguide bends. (a) shows the scattering at the input side of the MZI interferometer. (b) shows the scattering at the output side of the MZI interferometer.

Scattering losses clearly contribute to the total loss of the modulator device, which gives rise to the low transmission. Therefore, no output light can be detected. The scanning electron microscope (SEM) picture shows waveguides at bends (Fig.5.17 (b)) and the Y-junction (Fig.5.17 (c)).

The roughness on the bent waveguides can be seen in the SEM picture, which results in strong scattering during the measurement. As the losses are too high and no light through the modulators could be detected, a voltage dependent transmission measurement could not be performed.



(a) **(b)**



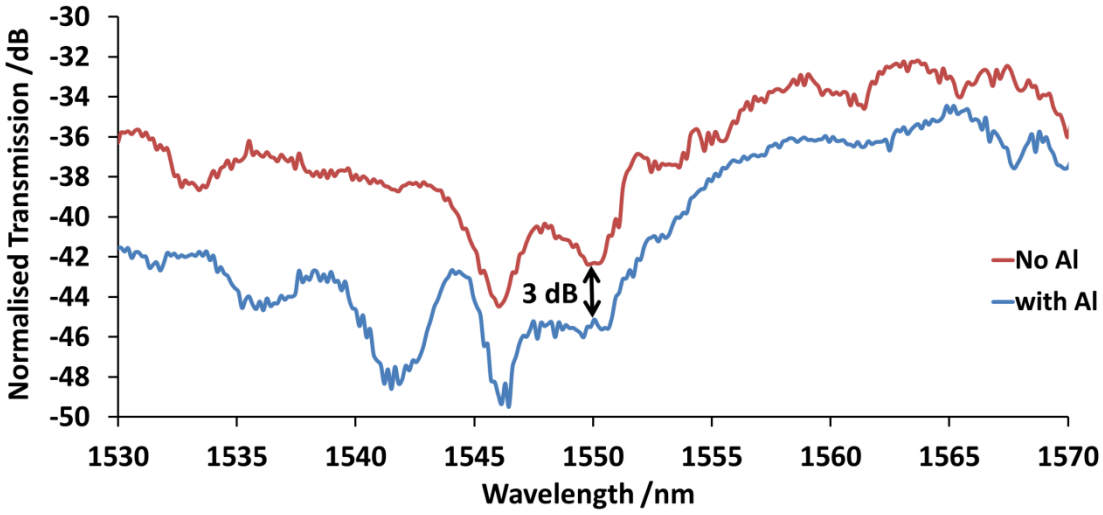
(c)

Fig.5.17 SEM picture of bends (b) and a Y-junction (c) showing the sidewall roughness. (b) and (c) are the magnified picture of the areas in (a). The waveguide sidewall roughness appears in (b) causes serious optical losses.

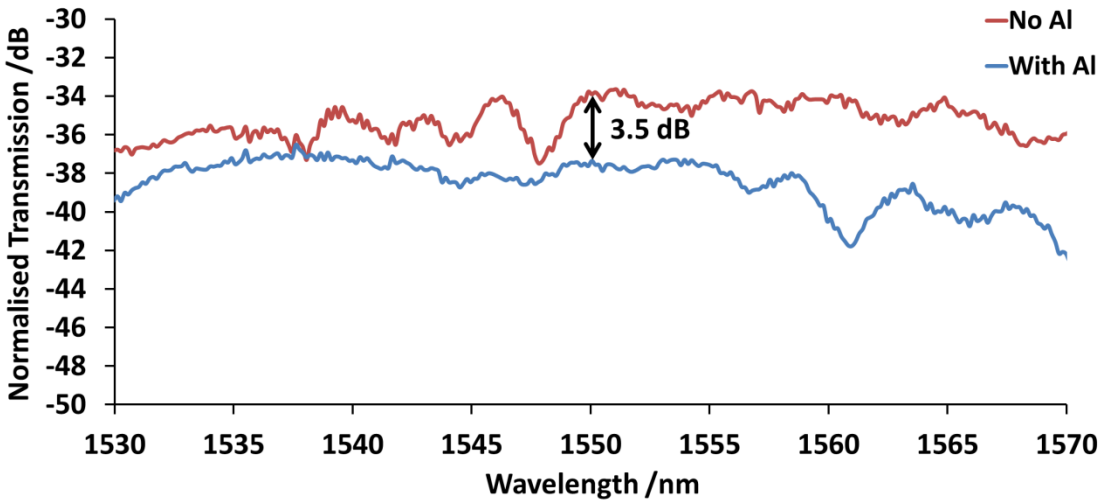
5.2.3 Al-FOx phase shifter

Finally, a phase shifter with thick FOx and Al contact was fabricated in comparison with the ITO-FOx phase shifter. The FOx layer is 300 nm thick in order to isolate the waveguide fully from the lossy Al contact. The undiluted FOx 14 was spun on the sample at 2000 rpm for 1 minute in order to achieve the desired thickness of 300 nm. A layer of aluminium with a thickness of 200 nm was used as the central contact. Otherwise, the design and fabrication process of the Al-FOx phase shifter is the same as that of the ITO-FOx phase shifter.

Before conducting voltage-dependent experiments, optical loss due to the Al central contact was assessed. Straight PhC waveguides with and without Al central contact were fabricated and measured. Fig.5.18 shows that the optical loss due to the Al central contact is over 3 dB depending on the wavelength.



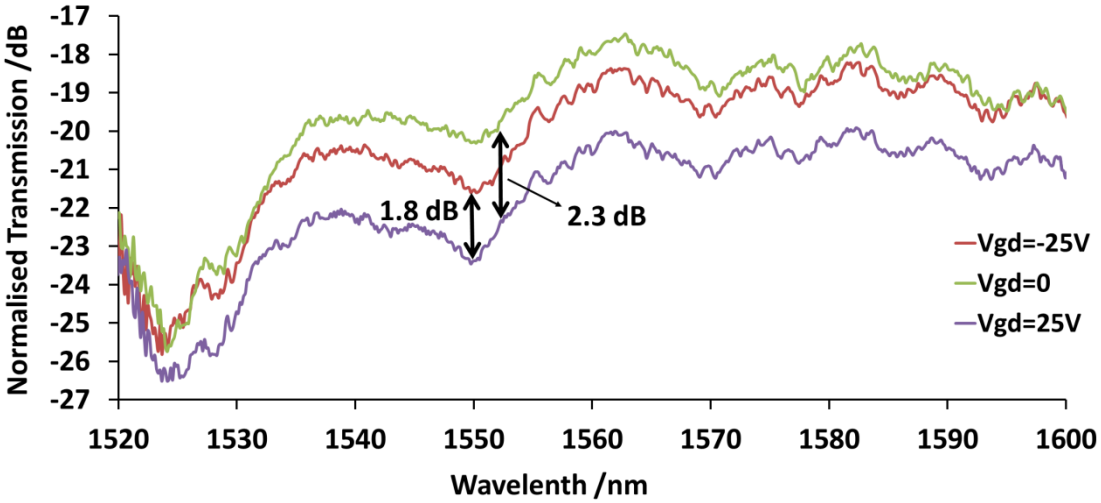
(a) Optical loss on PhC400 waveguides with 300 nm FOx due to Al central contact



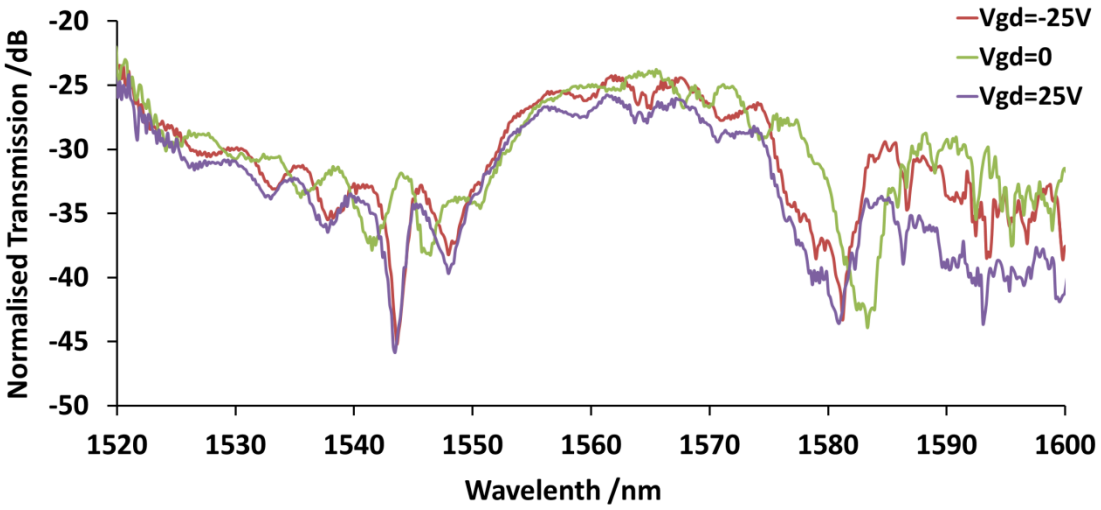
(b) Optical loss on PhC410 waveguides with 300 nm FOx due to Al central contact

Fig.5.18 Optical loss on PhC waveguides due to Al central contact. The loss due to Al contact is over 3 dB on 300 nm FOx layer.

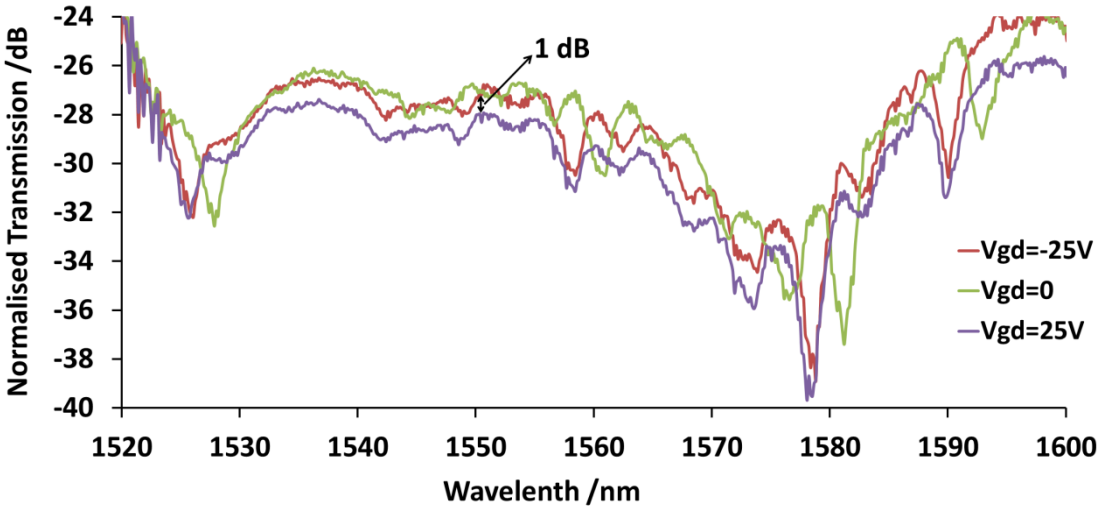
Then, voltages were applied to the Al central contact, and transmission of the Al-FOx phase shifters was measured. Three types of phase shifters, i.e. a blank waveguide phase shifter, a PhC400 phase shifter and a PhC410 phase shifter were measured. The results are shown in Fig.5.19.



(a) Normalised transmission spectra of blank waveguide phase shifter at different voltages



(b) Normalised transmission spectra of PhC400 phase shifter at different voltages



(c) Normalised transmission spectra of PhC410 phase shifter at different voltages

Fig.5.19 Al-FOx phase shifter transmission spectra measurement at different voltages showing loss change (over 1 dB) and spectra pattern shift.

Measurement was conducted with the two side contacts grounded. The voltages applied to the Al central contact are -25 V, 0 V and +25 V. Higher voltages broke down the FOx layer [54]. The change of transmission with applied voltages is quite clear. Transmission at -25 V and 0 V is higher than that at +25 V. At +25 V, the majority carrier in n-type silicon, electrons, accumulate in the waveguide, which increases the loss due to free carrier absorption. At -25 V, some electrons have been depleted from the waveguide. Therefore, the waveguide region has lower carrier density, which means smaller free carrier absorption. Transmission at 0 V is similar to that at -25 V. Moreover, transmission pattern shifts between different voltages, due to the change of refractive index. This can be observed most prominently for the photonic crystal samples.

In comparison with the ITO-FOx phase shifter, the Al-FOx phase shifter shows better performance. Although the loss changed by the applied voltage is low (1 dB at 50 V), the voltage applied transmission measurement result of the Al-FOx phase shifter demonstrates that the phase shifter design is correct and that it could generate electrically modulated phase change.

5.3 Discussion & conclusion

Although the MZI structure shows some interference response after depositing ITO on both arms and thus balancing the losses, the transmission of the complete device, including Al contacts, cannot be measured due to very large overall losses. There are three reasons for the strong losses. The first is absorption loss from ITO. Measurements show that ITO loss is 7 - 8 dB in minimum, which greatly depends on the fabrication process, especially on deposition and annealing. The second loss source is the fabrication process of FOx etching and Al contacts. In these fabrication processes, there were two thermal process steps of baking at 180˚C for 10 minutes and 5 minutes, respectively. Two photoresists, ZEP 520A and diluted PMMA 950K were used. Three solvents, 1165, acetone and IPA were used for cleaning and two developers, Xylene and MF319 were also used. The sample was etched in CHF_3 RIE for 10 minutes and Al was deposited by the thermal evaporator. Additional optical losses must arise from these processes, although this is not fully understood. The third source of loss is the sidewall roughness on the Y-junction and bent waveguides. We observed serious sidewall roughness on the bent waveguides, which increased

losses significantly. Due to all these losses, optical power passing through the modulator was too low to measure.

The second major issue is that in the Voltage applied optical transmission measurement, loss change due to carrier density change is very small. This may be because the electric field applied to the phase shifter was too weak. Therefore, the effect of carrier density change was not strong enough to significantly affect the optical loss due to free carrier absorption. Larger voltages and longer phase shifters could solve this problem and achieve a π phase change. Nevertheless, higher voltages break down the thin ITO film and in any case, high Voltage operation was not the goal of this work, as it is not possible to drive such high voltages at GHz speeds.

Another possible improvement could be to anneal the side Al contacts. Thermal annealing helps to reduce Al contact resistance, which would also improve the electrical performance of the phase shifter.

The Al-FOx phase shifters worked successfully. Transmission patterns shifted with the applied voltage, as the refractive index was electrically modulated. Test results of the Al-FOx phase shifter indicate that the phase shifter design is correct. The ITO-FOx phase shifter has the same structure as the Al-FOx phase shifter. The reason why the ITO-FOx phase shifter does not work as well can be attributed to ITO and its properties. Essentially, ITO is a semiconductor. Its electrical conduction comes from the dopants. Usually, the carrier concentration of ITO is over 10^{20} cm^{-3} to get a suitable conductivity. However, the same high carrier density also causes high optical losses, so it is not possible to reduce optical loss due to free carrier

absorption to zero as long as electrical conduction is required. Therefore, the best compromise is to keep a balance between electrical conductivity and optical transparency. However, this is not easy and requires advanced fabrication technology to precisely control all factors in the ITO fabrication process.

Chapter 6

Conclusion and Future Work

In this work, an ITO-FOx phase shifter and a silicon electro-optic MZI modulator incorporating a phase shifter have been fabricated and investigated. A similar phase shifter based on Al and FOx has also been demonstrated. ITO properties and fabrication techniques have been studied and Al contact to silicon has been investigated and tested.

The modulators have exhibited an MZI interference pattern, but the output optical power is very weak. Results from the Al-FOx phase shifter indicate that the optical transmission of the phase shifter is modulated by an applied voltage. The transmission pattern also shifts with applied voltages due to the electrically modulated refractive index in the phase shifter waveguide. The MOS capacitor working as a carrier operator changes the carrier density as well as the refractive index with applied voltages. For high speed modulation, further investigations of the device RC constant, electrical driving scheme and doping levels are needed.

Although the ITO-FOx phase shifter, and the modulator based on it, both fail to operate satisfactorily, a lot has been learned about this type of device. The main reason is high optical losses due to silicon waveguide sidewall roughness and fabrication process. ITO as a transparent conducting material is still promising to use in the modulator in terms of keeping metal contacts away from the silicon waveguide and consequently lowering the optical loss due to metal absorption. Given the following improvement, the device based on ITO could be made to work. Firstly, strong scattering from the Y-junctions and bent waveguides has been observed due to the sidewall roughness. Improved electron-beam lithography techniques can be applied to reduce the sidewall roughness. By using Multi-mode interferometer (MMI) couplers and bent waveguides with a larger radius instead of the current Y-junctions and bends, the optical loss can be lowered.

Secondly, to improve the electrical performance of the phase shifter, a highly doped silicon substrate can be used to reduce the contact resistance. Also, instead of Al contact, nickel silicide contacts can be used, as they typically have lower contact resistance. If Al contacts continue to be used, rapid thermal annealing could be used to decrease the contact resistance. Moreover, by using high resolution photolithography and electron-beam lithography, the side contacts could be fabricated closer to the central contact, which reduces the RC constant of the device even further. With the contact resistance decreasing, the electrical performance of the phase shifter improves.

Thirdly, advanced ITO deposition techniques can be used to control the electrical and optical properties of ITO better. Sputtering and pulsed laser deposition

are the most popular techniques to deposit ITO films, which can control tin dopant proportion during the deposition process and have better film quality. As free carriers arise from dopants, a lower doping level means lower free carrier concentration and consequently, lower free carrier absorption. Gases such as O_2 can be used during the deposition process to make the ITO films well oxidized. Substrate heating during the deposition is another widely used technique, which can improve the ITO oxidation and crystallization. All these techniques can control the carrier concentration and mobility of ITO film, which are the key factors that determine the electrical and optical properties of ITO.

Fourthly, instead of making the Al contact and ITO electrode directly on top of the waveguide region, they should be moved to the side and away from the waveguides (see Fig.6.1). In this way, the optical losses due to metal absorption can be eliminated. Besides, the ITO layer can be very thin in this configuration, as the optical isolation in vertical direction is no longer needed. Consequently, optical losses due to free carrier absorption in the ITO film can be further reduced. Moreover, in such a design, the FOx layer as a gate oxide can also be made thinner, which lowers the driving voltage and improves the electrical performance of the MOS capacitor phase shifter. In the structure shown in Fig.6.1, the thicknesses of the ITO and SiO_2 can be less than 100 nm. SiO_2 is only used as a gate oxide to form the MOS capacitor and the ITO is used to transfer the applied electric field from the Al contact to the gate oxide.

Besides, by using the transparent conductor, Al central contact can be far away from the optical mode (Fig.3.2), which greatly eliminates the optical loss due to

metal absorption. Moreover, moving the Al contact to the side decreases the thicknesses of the transparent conductor and SiO_2, as the optical isolation in the vertical direction is no longer needed in this situation. Thus, the driving voltage can be further reduced. In the structure shown in Fig.3.2, the thicknesses of the ITO and SiO_2 can be less than 100 nm. SiO_2 is only used as a gate oxide to form the MOS capacitor and the ITO is used as a transparent electrode to transfer the applied voltage from the Al contact to the gate oxide.

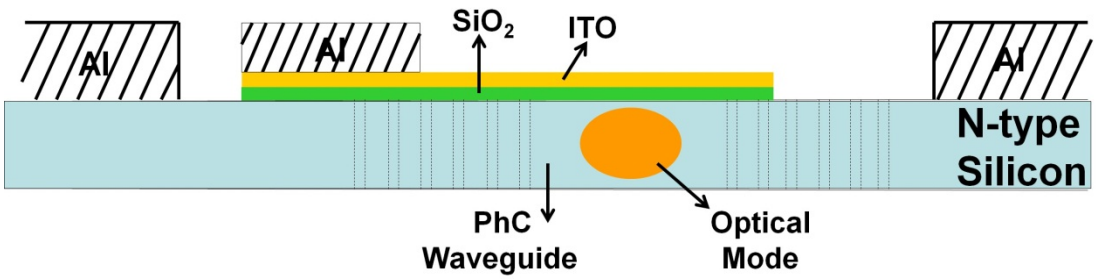


Fig.6.1 Cross-sectional view of the silicon MOS capacitor phase shifter with the central Al contact moving to the side. In this structure (Al/ITO/SiO_2/Si), as Al central contact is moved to the side and away from the waveguide region, the thicknesses of the ITO and SiO_2 can be reduced to less than 100 nm. Therefore, optical losses due to Al central contact and ITO film can be minimized.

As the modulator failed to operate satisfactorily, there was no opportunity to employ slow light enhancement of the engineered PhC waveguide to enhance sensitivity. However, this is a promising property to use in future silicon electro-optic modulator development, as the slow light enhancement could reduce the phase shifting length.

In conclusion, this work demonstrates that the asymmetric MZI structure of the modulator shows the interference pattern. The Al-FOx phase shifter shows the loss change due to applied voltages, which indicates the free carrier density is modified by the applied electric field. Although in this research the ITO-FOx phase shifters did not work due to the high optical losses, ITO still showed promise to use in silicon electro-optic modulators as an isolation layer to separate silicon waveguides from Al contacts. This lowers the optical losses due to metal absorption. Slow light photonic crystal waveguides are quite powerful to use in the modulator in terms of shortening the phase shifter length. For future work, improvements need to be done to lower the entire optical loss of the modulator and especially, advanced fabrication technologies are needed to improve the modulator fabrication process to achieve better performance.

Appendix

Scripts for Synopsys TCAD Simulations

The Script of Sentaurus Device Simulation

```
*DC Modelling: MOS capacitor phase shifter 3D simulation
*Silicon P Type Doping Concentration: 3e17 cm^-3
*SiO2 Thickness: 100 nm
*DC Gate Voltage:0-25 V

Device Modulator{

*Defining Electrode Name & Preset Voltage
Electrode{
{ Name="Gate"                   Voltage=0.0     }
{ Name="Ground_left"            Voltage=0.0     }
{ Name="Ground_right"           Voltage=0.0     }
        }

File{
*Input Files:
Grid= "sdevice_msh.tdr"
Parameter= "sdevice.par"

*Output Files:
Plot="DC"
Current="DC"
    }

*Physics Models Used in Modulator Simulations
Physics{
Hydrodynamic
EffectiveIntrinsicDensity(BandGapNarrowing (OldSlotboom))
RecGenHeat
Fermi
      }

*Physics Models of Silicon Material
Physics(Material="Silicon"){
                        eQuantumPotential       hQuantumPotential
                        Mobility(
                                PhuMob
                                eHighFieldSaturation(CarrierTempDrive)
```

```
                    hHighFieldSaturation(CarrierTempDrive)
                    Enormal
                    )
                Recombination(
                SRH( DopingDep )
                Band2Band
                        )
                }
        }
```

```
*Settings of Exported Values for Plotting
Plot{
*--Density and Currents, etc
eDensity hDensity
TotalCurrent/Vector eCurrent/Vector hCurrent/Vector
eMobility hMobility
eTemperature hTemperature

*--Fields and charges
ElectricField/Vector Potential SpaceCharge

*--Doping Profiles
Doping DonorConcentration  AcceptorConcentration

*--Generation/Recombination
SRH Band2Band

* Auger AvalancheGeneration
eAvalancheGeneration        hAvalancheGeneration
SRHRecombination

*--Band structure/Composition
BandGap
BandGapNarrowing
Affinity
ConductionBandValenceBand
eQuantumPotential
  }

*Settings for Mathematical Calculation
Math {
Digits=10
Extrapolate
Iterations=20
Notdamped =50
RelErrControl
```

```
ErrRef(Electron)=1.e10
ErrRef(Hole)=1.e10
ExtendedPrecision
RhsMin=1e-20
NoAutomaticCircuitContact
        }


*The Computation Process
Solve {
#- Creating initial guess:
Coupled(Iterations=100 LineSearchDamping=1e-4){ Poisson eQuantumPotential
hQuantumPotential }
Coupled{ Poisson eQuantumPotential hQuantumPotential Electron Hole }
Coupled{ Poisson eQuantumPotential hQuantumPotential Electron Hole
eTemperature hTemperature }

#- Vg sweep DC Analysis
NewCurrentFile="DC_"
Quasistationary(
*     InitialStep=0.1 Increment=2
*     MinStep=1e-6  MaxStep=0.8
Goal{ Name="Gate" Voltage=@Vgmin@ }
                    )
{Coupled{ Poisson eQuantumPotential hQuantumPotential Electron Hole
eTemperature hTemperature }
CurrentPlot(Time=(Range=(0 1) Intervals=@NumP_DC@))
Plot(FilePrefix="DC" NoOverWrite)
}
      }
```

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